# Compal Confidential

## BIUS1/S2 & BIUY0/Y1
## DIS M/B Schematics Document

### Intel SkyLake U Processor with DDR4
### AMD R16M-M1-30/R16M-M2-50

2016-02-16

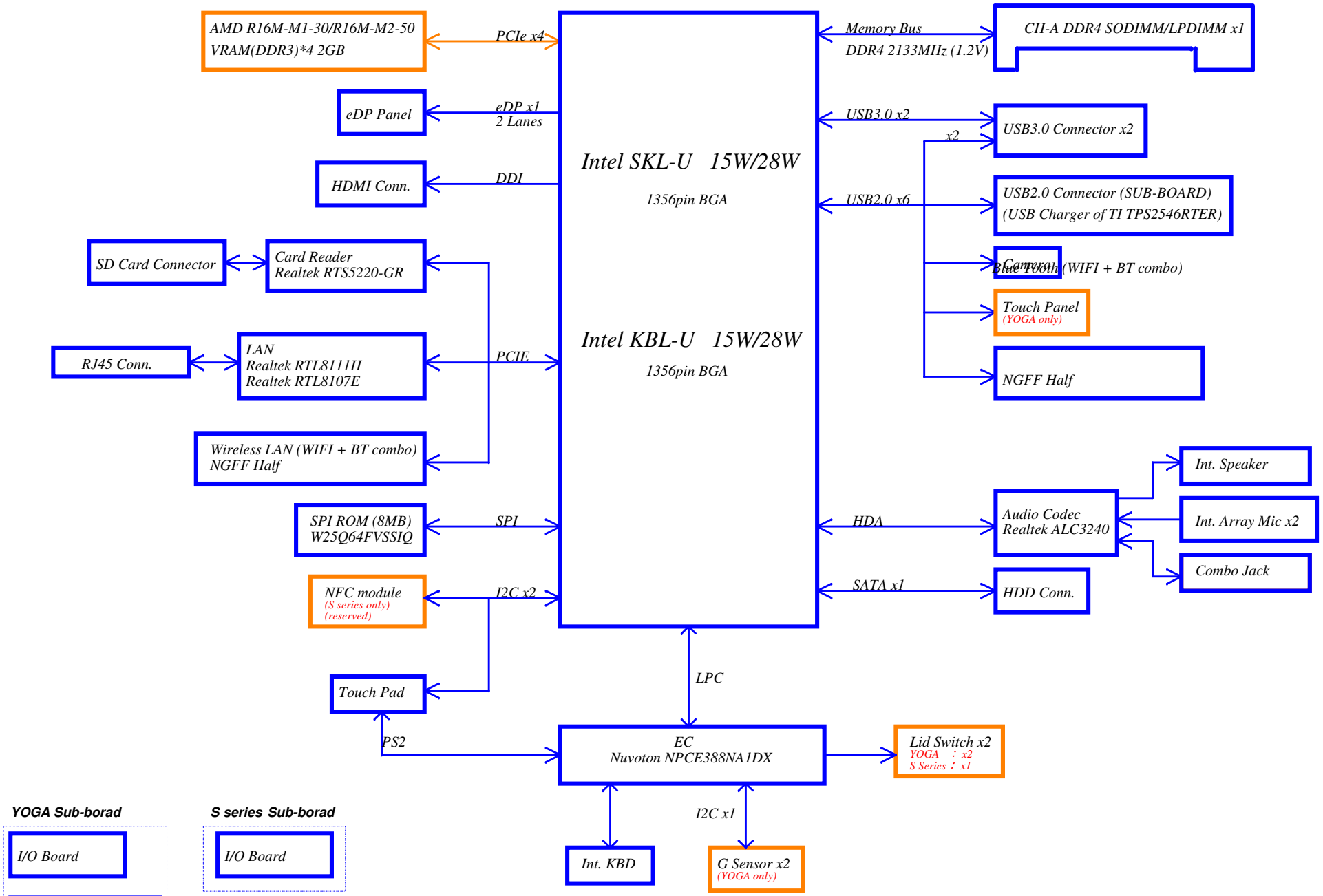
LA-D451P

REV：1.0



| | | |
|---|---|---|
| Compal Electronics, Inc. | | |
| Title: Cover Page | | |
| Size: C | Document Number: LA-D451P | Rev: 1.0 |
| Date: Tuesday, February 16, 2016 | Sheet 1 of 50 | |

# YOGA/S series

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| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |
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## Voltage Rails

| power plane / State | B+ | +5VALW<br>+3VALW | +1.5V | +5VS<br>+3VS<br>+1.35VS<br>+1.0VS_VCCOPC<br>+VCC_CORE<br>+VGA_CORE<br>+VCC_GFXCORE_AXG<br>+1.8VS<br>+0.75VS<br>+1.0VALW |
|---|---|---|---|---|
| S0 | O | O | O | O |
| S3 | O | O | O | X |
| S5 S4/AC | O | O | X | X |
| S5 S4/ Battery only | O | X | X | X |
| S5 S4/AC & Battery don't exist | X | X | X | X |

## BOM Structure Table

| Item | BOM Structure |
|---|---|
| LAN 10/100 Transformer | 100@ |
| LAN Giga Transformer | GIGA@ |
| For Giga LAN Chip | 8111H@ |
| For 10/100 LAN Chip | 8107E@ |
| For DIS | DIS@ |
| For UMA | UMA@ |
| For GPU M1 Chip | M1@ |
| For GPU M2 Chip | M2@ |
| For NFC Option | NFC@ |
| For Thermal Chip | EX_THM@ |
| For Keyboard backlight | KBL@ |
| No Keyboard backlight | NOKBL@ |
| For Hynix Memory | H2G@ |
| For Samsung Memory | S2G@ |
| For Micron Memory | M2G@ |
| For EMI | EMI@ |
| For ESD | ESD@ |
| No EMI | @EMI@ |
| No ESD | @ESD@ |
| Connector | ME@ |
| For VARM X76 | GM_X76@ |
| For Test Point | TP@ |
| For 2+3E power | 23E@ |
| For S series only | SS@ |
| For YOGA series only | YOGA@ |
| For 14 inch only | 14@ |
| For 15 inch only | 15@ |
| For CPU Type | 6500U@ |
| | 6200U@ |
| | 6100U@ |
| | 4405U@ |

## EC SM Bus1 address

| Device | Address |
|---|---|
| Smart Battery | 0001 011x 16h |

## EC SM Bus2 address

| Device | Address |
|---|---|
| NCT7718W | 1001 100x 98h |

## EC SM Bus4 address

| Device | Address |
|---|---|
| BMA250E | 0001 100X 18h |

## ME SM Bus address

| Device | Address |
|---|---|
| NFC | 0010 1000 28h |

## PCH SM Bus address

| Device | Address |
|---|---|
| DDR_JDIMM1<br>Touch Pad | 1010 000x A0h |

## GPU SM Bus address

| Device | Address |
|---|---|
| Internal thermal sensor | 1001 111x 9Eh |

# Vinafix

## USB 2.0 Port Table

| Port | External USB Port |
|---|---|
| 1 | Touch panel (for YOGA only) |
| 2 | USB2/3 MB(JUSB1) |
| 3 | USB2/3 MB(JUSB2) |
| 4 | USB2 IO Board(Charger) |
| 5 | Camera |
| 6 | |
| 7 | NGFF WLAN+BT |

## USB 3.0 Port Table

| Port | |
|---|---|
| 1 | |
| 2 | USB2/3 MB(JUSB1) |
| 3 | USB2/3 MB(JUSB2) |
| 4 | |
| 5 | |
| 6 | |

## SATA Port Table

| Port | |
|---|---|
| 0 | HDD |
| 1 | |

## PCIE Port Table

| Port | Lane | |
|---|---|---|
| 1 | 1 | GPU |
| 2 | 2 | |
| 3 | 3 | |
| 4 | 4 | |
| 5 | | LAN |
| 6 | | NGFF WLAN+BT |
| 7 | | |
| 8 | | |
| 9 | | |
| 10 | | |

## SMBUS Control Table

| | SOURCE | VGA | BATT | CHARGER | NECP388 | SODIMM | Thermal Sensor | DGPU | CRT RT2168 | NFC | TP | PCH | G-SENSOR |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SMB_EC_CK1<br>SMB_EC_DA1 | NECP388<br>+3VALW | X | V<br>+3VALW | V<br>+19V_VIN | X | X | X | X | X | X | X | X | X |
| SMB_EC_CK2<br>SMB_EC_DA2 | NECP388<br>+3VS | V<br>+3VGS | X | X | V<br>+3VS | X | V<br>+3VS | X | X | X | X | V<br>+3VS | X |
| SMB_EC_CK4<br>SMB_EC_DA4 | NECP388<br>+3VALW | X | X | X | X | X | X | X | X | X | X | X | V<br>+3VS |
| PCH_SMBCLK<br>PCH_SMBDATA | PCH<br>+3VALW | X | X | X | X | V<br>+3VS | X | X | X | X | V<br>+3VS | X | X |
| SML0CLK<br>SML0DATA | PCH<br>+3VALW | X | X | X | X | X | X | X | X | V<br>+3VS | X | X | X |
| SML1CLK<br>SML1DATA | PCH<br>+3VALW | X | X | X | V<br>+3VS | X | X | V<br>+3VS | X | X | X | X | X |

| STATE / SIGNAL | SLP_S1# | SLP_S3# | SLP_S4# | SLP_S5# | +VALW | +V | +VS | Clock |
|---|---|---|---|---|---|---|---|---|
| Full ON | HIGH | HIGH | HIGH | HIGH | ON | ON | ON | ON |
| S1(Power On Suspend) | LOW | HIGH | HIGH | HIGH | ON | ON | ON | LOW |
| S3 (Suspend to RAM) | LOW | LOW | HIGH | HIGH | ON | ON | OFF | OFF |
| S4 (Suspend to Disk) | LOW | LOW | LOW | HIGH | ON | OFF | OFF | OFF |
| S5 (Soft OFF) | LOW | LOW | LOW | LOW | ON | OFF | OFF | OFF |



| | | | |
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Title: Notes List

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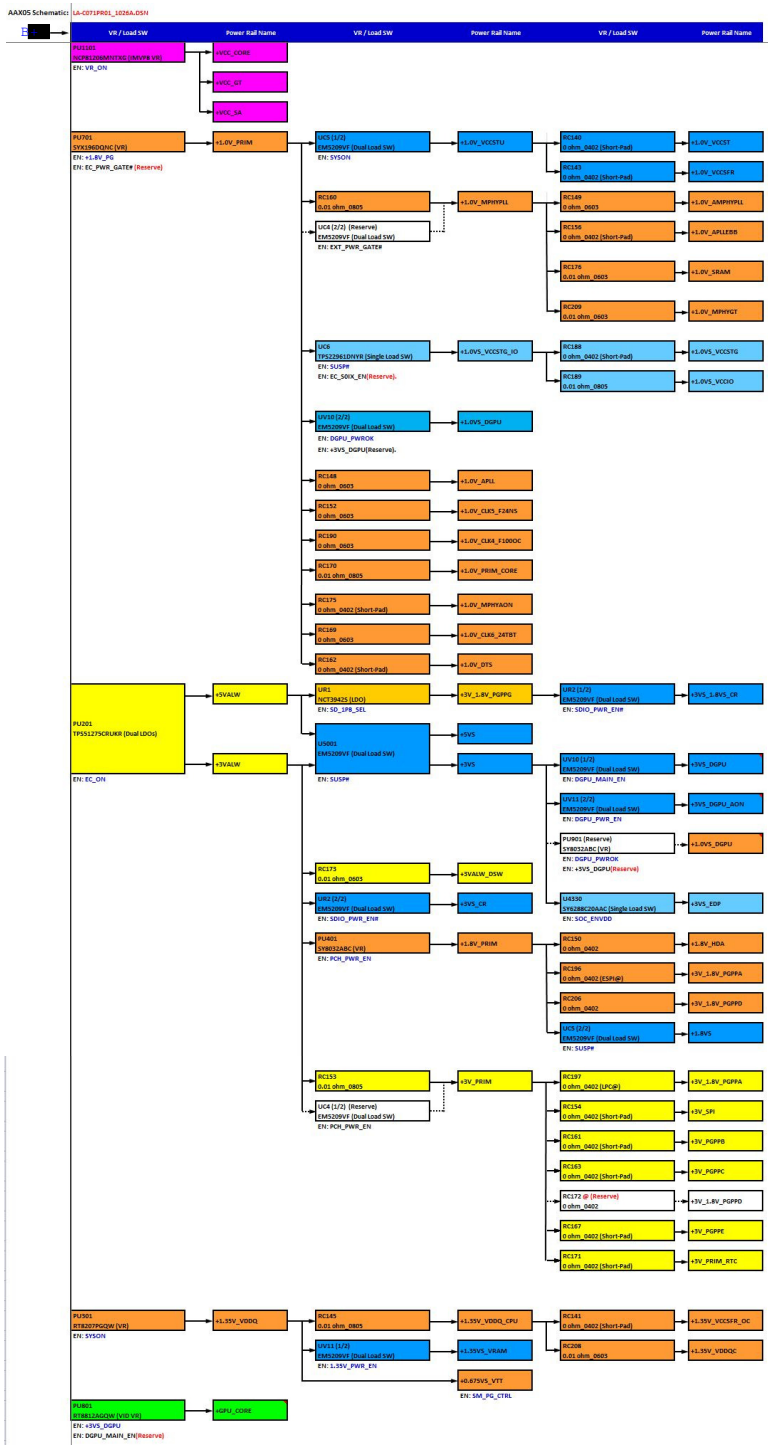
# BIVS3/ VE3 -PowerMap_SKL-U22_DDR3L_Volume_NON CS]

AAX05 Schematics: LA-C071PR01_1026A.DSN

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|---|---|---|---|
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |



**Compal Electronics, Inc.**

Title: **Power MAP**

| Size | Document Number | Rev |
|---|---|---|
| | | 1.0 |

Date: Tuesday, February 16, 2016 Sheet 4 of 50

## [AAX05-PWR Sequence_SKL-U22_DDR3L_Volume_NON CS]


| | | | |
|---|---|---|---|
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**Compal Electronics, Inc.**

Title: **Power Sequence**

| Size | Document Number | Rev |
|---|---|---|
| | | 1.0 |

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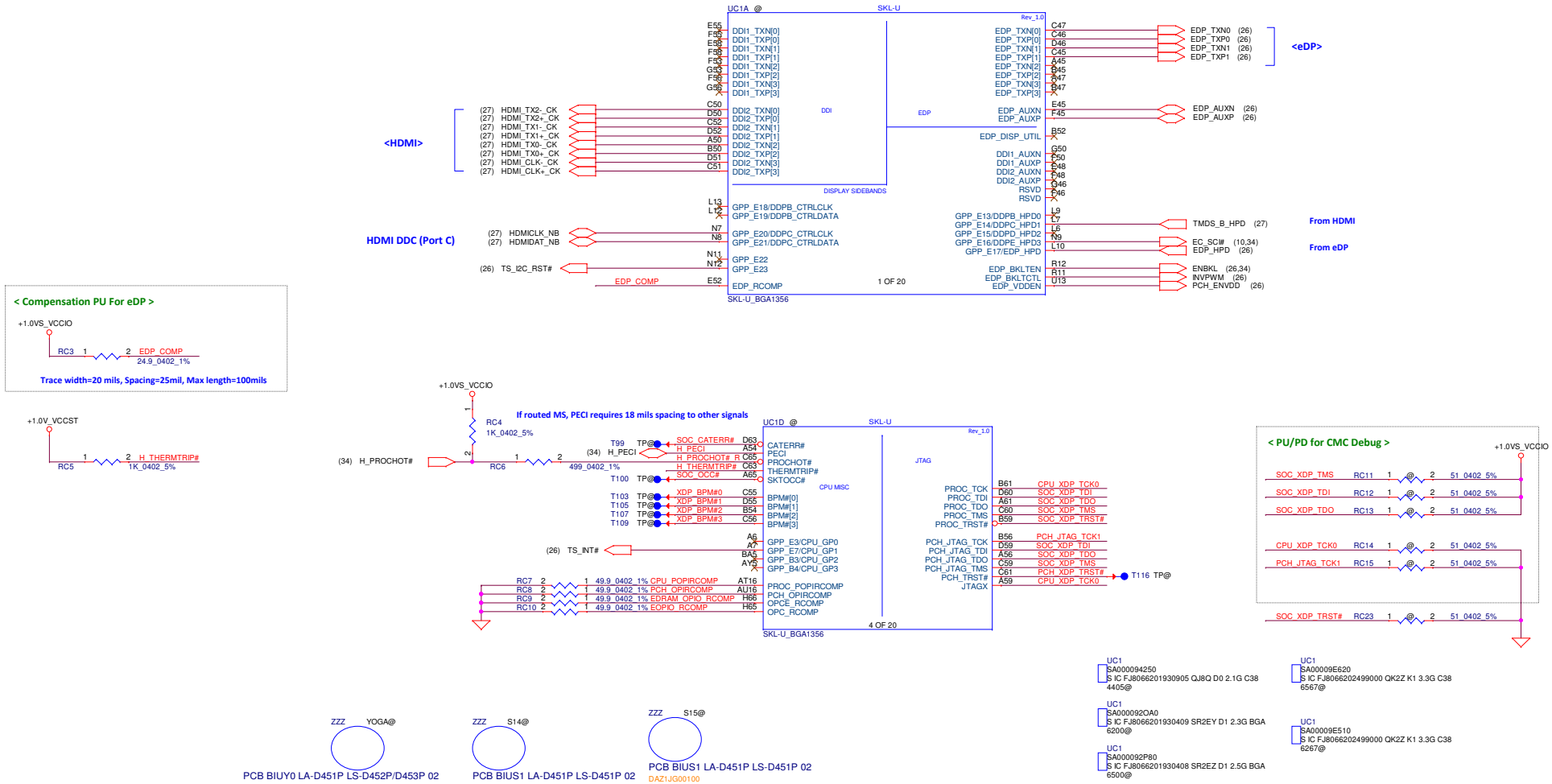


| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |



Compal Electronics, Inc.

Title: SKL-U(1/12)DDI,EDP,MISC,CMC

| Size | Document Number | Rev |
|---|---|---|
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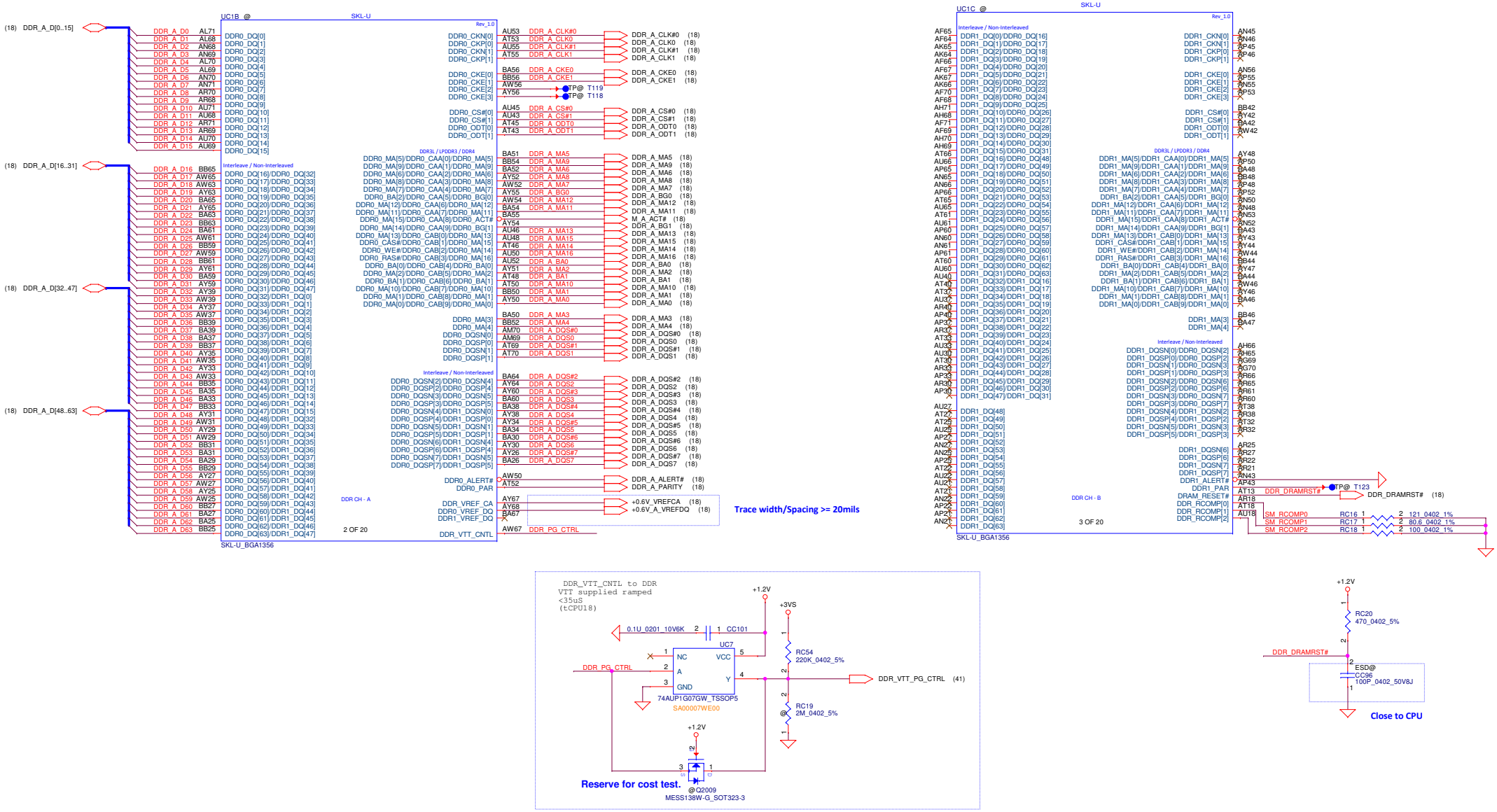
# Interleaved Memory




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |



| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title | SKL-U(2/12)DDR3L | | |
| Size: Custom | Document Number: LA-D451P | | Rev: 1.0 |
| Date: Tuesday, February 16, 2016 | Sheet 7 of 50 | | |

SML0ALERT# (Internal Pull Down):

eSPI or LPC

0 = LPC is selected for EC ==> Default

1 = eSPI is selected for EC

+3VS

RC112 1 2 10K_0402_5% KB_RST#

+3VALW

RC21 1 @ 2 1K_0402_5% SOC_SPI_IO2

RC22 1 @ 2 1K_0402_5% SOC_SPI_IO3

RC24 1 @ 2 1K_0402_5%

From WW36 MOW for SKL-U ES sample

+1.8VS_3VS_PGPPA

RC25 1 2 8.2K_0402_5% SERIRQ

UC1E @ SKL-U Rev_1.0

SPI - FLASH

SOC_SPI_CLK AV2 SPI0_CLK

SOC_SPI_SO AW3 SPI0_MISO

SOC_SPI_SI AV3 SPI0_MOSI

SOC_SPI_IO2 AW2 SPI0_IO2

SOC_SPI_IO3 AU4 SPI0_IO3

SOC_SPI_CS#0 AU3 SPI0_CS0#

AU2 SPI0_CS1#

AU1 SPI0_CS2#

SPI - TOUCH

M2 GPP_D1/SPI1_CLK

M3 GPP_D2/SPI1_MISO

J4 GPP_D3/SPI1_MOSI

V1 GPP_D21/SPI1_IO2

V2 GPP_D22/SPI1_IO3

M1 GPP_D0/SPI1_CS#

C LINK

G3 CL_CLK

G2 CL_DATA

G1 CL_RST#

(34) KB_RST# KB_RST# AW13 GPP_A0/RCIN#

(34) SERIRQ SERIRQ AY11 GPP_A6/SERIRQ

SKL-U_BGA1356

5 OF 20

SMBUS, SMLINK

GPP_C0/SMBCLK R7 PCH_SMB_CLK PCH_SMB_CLK (18,32)

GPP_C1/SMBDATA R8 PCH_SMB_DATA PCH_SMB_DATA (18,32)

GPP_C2/SMBALERT# R10 SOC_SMBALERT# TP@ T124

GPP_C3/SML0CLK R9 SOC_SML0CLK SOC_SML0CLK (29)

GPP_C4/SML0DATA W2 SOC_SML0DATA SOC_SML0DATA (29)

GPP_C5/SML0ALERT# W1 SOC_SML0ALERT# TP@ T125

GPP_C6/SML1CLK W3

GPP_C7/SML1DATA V3 EC_SMB_CK2 (20,31,34)

GPP_B23/SML1ALERT#/PCHHOT# AM7 SOC_SML1ALERT# EC_SMB_DA2 (20,31,34)

LPC

GPP_A1/LAD0/ESPI_IO0 AY13 LPC_AD0 LPC_AD0 (34)

GPP_A2/LAD1/ESPI_IO1 BA13 LPC_AD1 LPC_AD1 (34)

GPP_A3/LAD2/ESPI_IO2 BB13 LPC_AD2 LPC_AD2 (34)

GPP_A4/LAD3/ESPI_IO3 AY12 LPC_AD3 LPC_AD3 (34)

GPP_A5/LFRAME#/ESPI_CS# BA12 LPC_FRAME# LPC_FRAME# (34)

GPP_A14/SUS_STAT#/ESPI_RESET# BA11

GPP_A9/CLKOUT_LPC0/ESPI_CLK AW9 LPC_CLK0 RC26 1 EMI@ 2 22_0402_5% CLK_LPC_EC (34)

GPP_A10/CLKOUT_LPC1 AY9

GPP_A8/CLKRUN# AW11 PM_CLKRUN#

SML0ALERT# (Internal Pull Down):

eSPI or LPC

0 = LPC is selected for EC ==> Default

1 = eSPI is selected for EC

SMB (Link to DDR,TP)

SML0 (Link to NFC)

SML1 (Link to EC,DGPU,Thermal Sensor)

RPC1, RPC3 and RC30 are close to UC3

From SOC

RPC1

SOC_SPI_SO 1 8 SOC_SPI_SO_0_R

SOC_SPI_CLK 2 7 SOC_SPI_CLK_0_R

SOC_SPI_SI 3 6 SOC_SPI_SI_0_R

SOC_SPI_IO3 4 5 SOC_SPI_IO3_0_R

33_0804_8P4R_5%

EMI@

SOC_SPI_IO2 1 RC30 EMI@ 2 SOC_SPI_IO2_0_R 33_0402_5%

From EC

(34) EC_SPI_CLK

(34) EC_SPI_MOSI

(34) EC_SPI_CS0#

(34) EC_SPI_MISO

RPC3

EC_SPICLK 1 8 SOC_SPI_CLK_0_R

EC_MOSI 2 7 SOC_SPI_SI_0_R

EC_SPICS# 3 6 SOC_SPI_CS#0

EC_MISO 4 5 SOC_SPI_SO_0_R

33_0804_8P4R_5%

EMI@

< SPI ROM - 8M >

+3VALW

UC3

SOC_SPI_CS#0 1 /CS VCC 8

SOC_SPI_SO_0_R 2 DO(IO1) /HOLD(IO3) 7 SOC_SPI_IO3_0_R

SOC_SPI_IO2_0_R 3 /WP(IO2) CLK 6 SOC_SPI_CLK_0_R

4 GND DI(IO0) 5 SOC_SPI_SI_0_R

W25Q64FVSSIQ_SO8

CC2 1 @ 2 0.1U_0201_10V K X5R

CC3 1 2 10P_0402_50V8J @EMI@

+3VS

SOC_SML0CLK 1 RC28 2 499_0402_1%

SOC_SML0DATA 1 RC29 2 499_0402_1%

SOC_SML1ALERT# 1 @ RC113 2 150K_0402_5%

RPC2

PCH_SMB_CLK 1 8

PCH_SMB_DATA 2 7

EC_SMB_CK2 3 6

EC_SMB_DA2 4 5

1K_0804_8P4R_5%

+1.8VS_3VS_PGPPA

PM_CLKRUN# 1 @ RC31 2 8.2K_0402_5%

Follow 543016_SKL_U_Y_PDG_0_9

| | | | |
|---|---|---|---|
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Title: SKL-U(3/12)SPI,SMB,LPC,ESPI

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< HD AUDIO >

(28) HDA_BITCLK_AUDIO
(28) HDA_SYNC_AUDIO
(28) HDA_SDOUT_AUDIO

RPC4
1 2 3 4 8 7 6 5
HDA_BIT_CLK
HDA_SYNC
HDA_SDOUT
33_0804_8P4R_5%
EMI@

< To Enable ME Override >

(34) ME_EN — RC116 2 1 0_0402_5% — HDA_SDOUT

UC1G @ SKL-U
Rev_1.0
AUDIO

(28) HDA_SDIN0
HDA_SYNC BA22
HDA_BIT_CLK AY22
HDA_SDOUT BB22
BA21
AY21
AW22
J5
AY20
AW20
HDA_SYNC/I2S0_SFRM
HDA_BLK/I2S0_SCLK
HDA_SDO/I2S0_TXD
HDA_SDI0/I2S0_RXD
HDA_SDI1/I2S1_RXD
HDA_RST#/I2S1_SCLK
GPP_D23/I2S_MCLK
I2S1_SFRM
I2S1_TXD

AK7
AK6
AK9
AK10
GPP_F1/I2S2_SFRM
GPP_F0/I2S2_SCLK
GPP_F2/I2S2_TXD
GPP_F3/I2S2_RXD

H5
D7
GPP_D19/DMIC_CLK0
GPP_D20/DMIC_DATA0

D8
C8
GPP_D17/DMIC_CLK1
GPP_D18/DMIC_DATA1

(28) HDA_SPKR — HDA_SPKR AW5 — GPP_B14/SPKR

SDIO / SDXC
GPP_G0/SD_CMD AB11
GPP_G1/SD_DATA0 AB13
GPP_G2/SD_DATA1 AB12
GPP_G3/SD_DATA2 W12
GPP_G4/SD_DATA3 W11
GPP_G5/SD_CD# W10
GPP_G6/SD_CLK W8
GPP_G7/SD_WP W7
GPP_A17/SD_PWR_EN#/ISH_GP7 BA9
GPP_A16/SD_1P8_SEL BB9
SD_RCOMP AB7 — RC76 1 @ 2 200_0402_1%
GPP_F23 AF13

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SKL-U_BGA1356

+3VS
RC33 1 @ 2 2.2K_0402_5% HDA_SPKR

SPKR (Internal Pull Down):

TOP Swap Override

0 = Disable TOP Swap mode. ==> Default

1 = Enable TOP Swap Mode.

UC1I @ SKL-U
Rev_1.0
CSI-2

A36 CSI2_DN0
B36 CSI2_DP0
C38 CSI2_DN1
D38 CSI2_DP1
C36 CSI2_DN2
D36 CSI2_DP2
A38 CSI2_DN3
B38 CSI2_DP3

C31 CSI2_DN4
D31 CSI2_DP4
C33 CSI2_DN5
D33 CSI2_DP5
A31 CSI2_DN6
B31 CSI2_DP6
A33 CSI2_DN7
B33 CSI2_DP7

A29 CSI2_DN8
B29 CSI2_DP8
C28 CSI2_DN9
D28 CSI2_DP9
A27 CSI2_DN10
B27 CSI2_DP10
C27 CSI2_DN11
D27 CSI2_DP11

CSI2_CLKN0 C37
CSI2_CLKP0 D37
CSI2_CLKN1 C32
CSI2_CLKP1 D32
CSI2_CLKN2 C29
CSI2_CLKP2 D29
CSI2_CLKN3 B26
CSI2_CLKP3 A26

CSI2_COMP E13 — RC80 1 @ 2 100_0402_1%
GPP_D4/FLASHTRIG B7

EMMC
GPP_F13/EMMC_DATA0 AP2
GPP_F14/EMMC_DATA1 AP1
GPP_F15/EMMC_DATA2 AP3
GPP_F16/EMMC_DATA3 AN3
GPP_F17/EMMC_DATA4 AN1
GPP_F18/EMMC_DATA5 AN2
GPP_F19/EMMC_DATA6 AM4
GPP_F20/EMMC_DATA7 AM1

GPP_F21/EMMC_RCLK AM2
GPP_F22/EMMC_CLK AM3
GPP_F12/EMMC_CMD AP4

EMMC_RCOMP AT1 — RC129 1 @ 2 200_0402_1%

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SKL-U_BGA1356



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Title: SKL-U(4/12)HDA,EMMC,SDIO,CSI2

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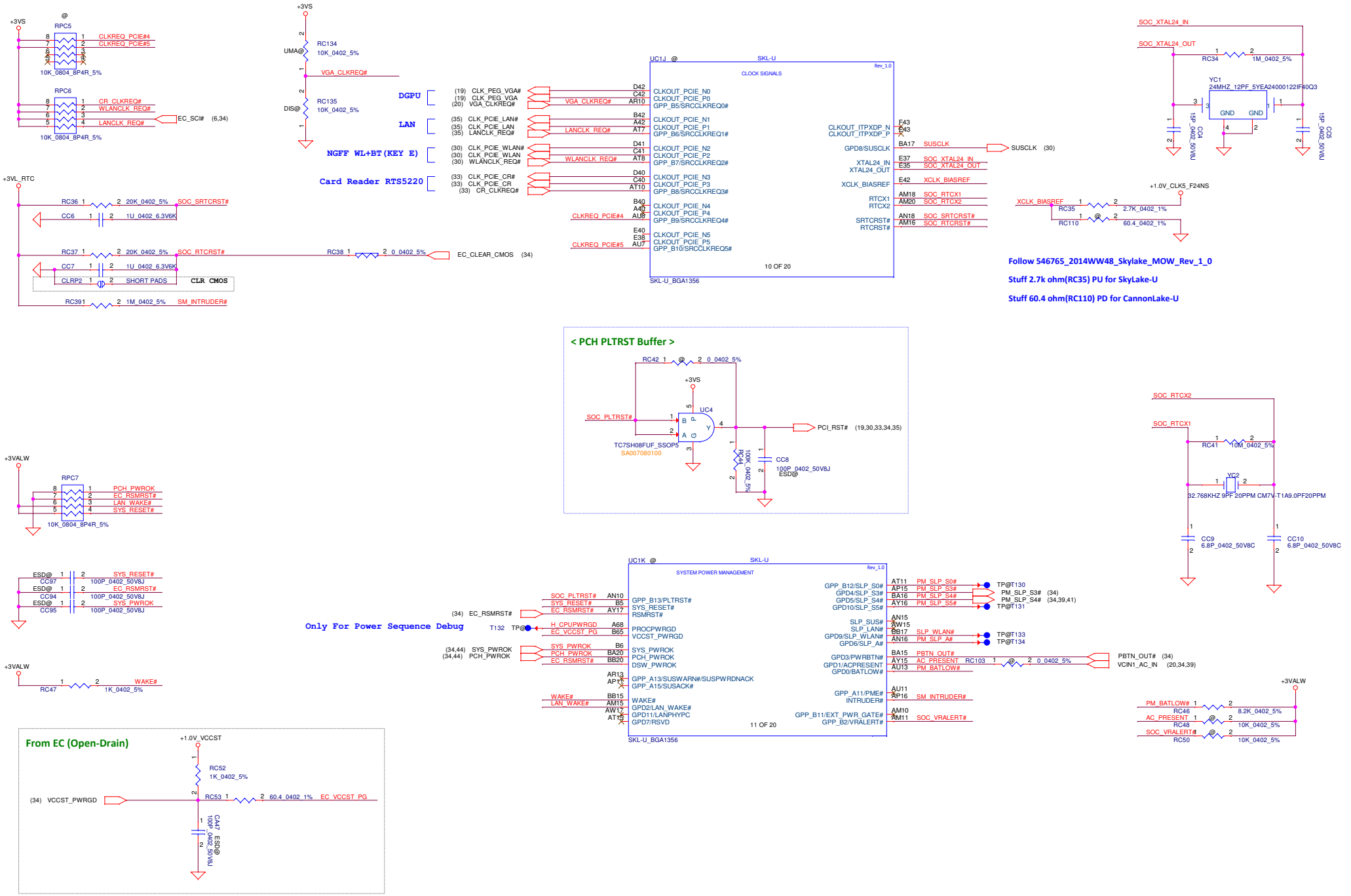


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|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |



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|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title | SKL-U(5/12)CLK,PM,GPIO | | |
| Size | Document Number | | Rev |
| Custom | LA-D451P | | 1.0 |
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**GSPI0_MOSI (Internal Pull Down):**

**No Reboot**

**0 = Disable No Reboot mode. ==> Default**

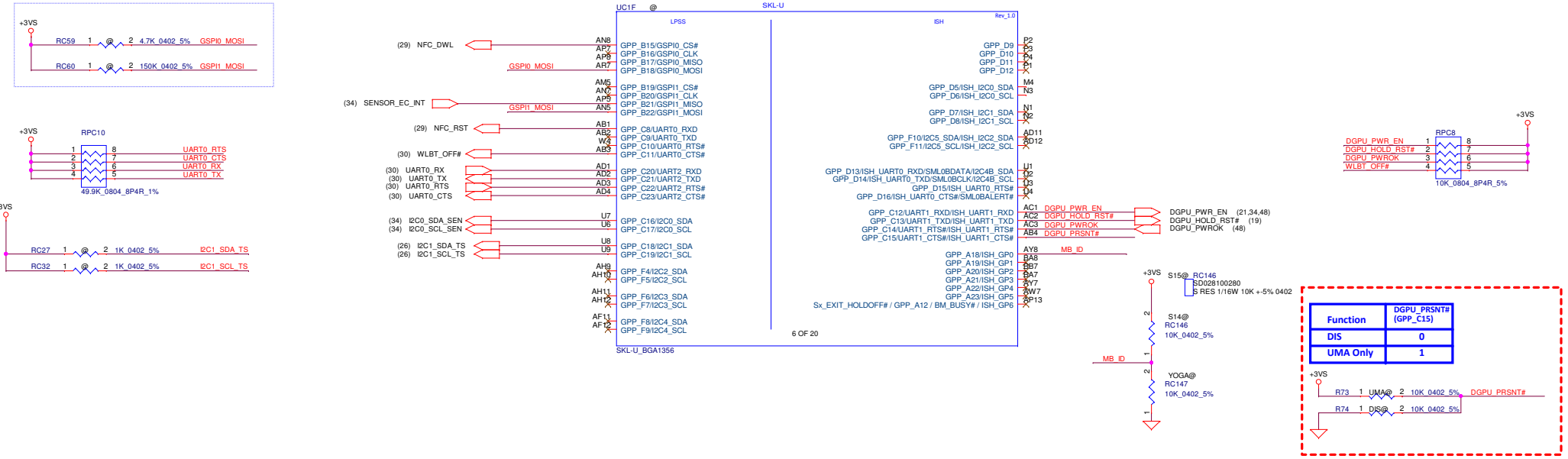
**1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.**

**GSPI1_MOSI (Internal Pull Down):**

**Boot BIOS Strap Bit**

**0 = SPI Mode ==> Default**

**1 = LPC Mode**

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|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |



Compal Electronics, Inc.

Title: SKL-U(6/12)GPIO,I2C,GSPI

| Size | Document Number | Rev |
|---|---|---|
| Custom | LA-D451P | 1.0 |

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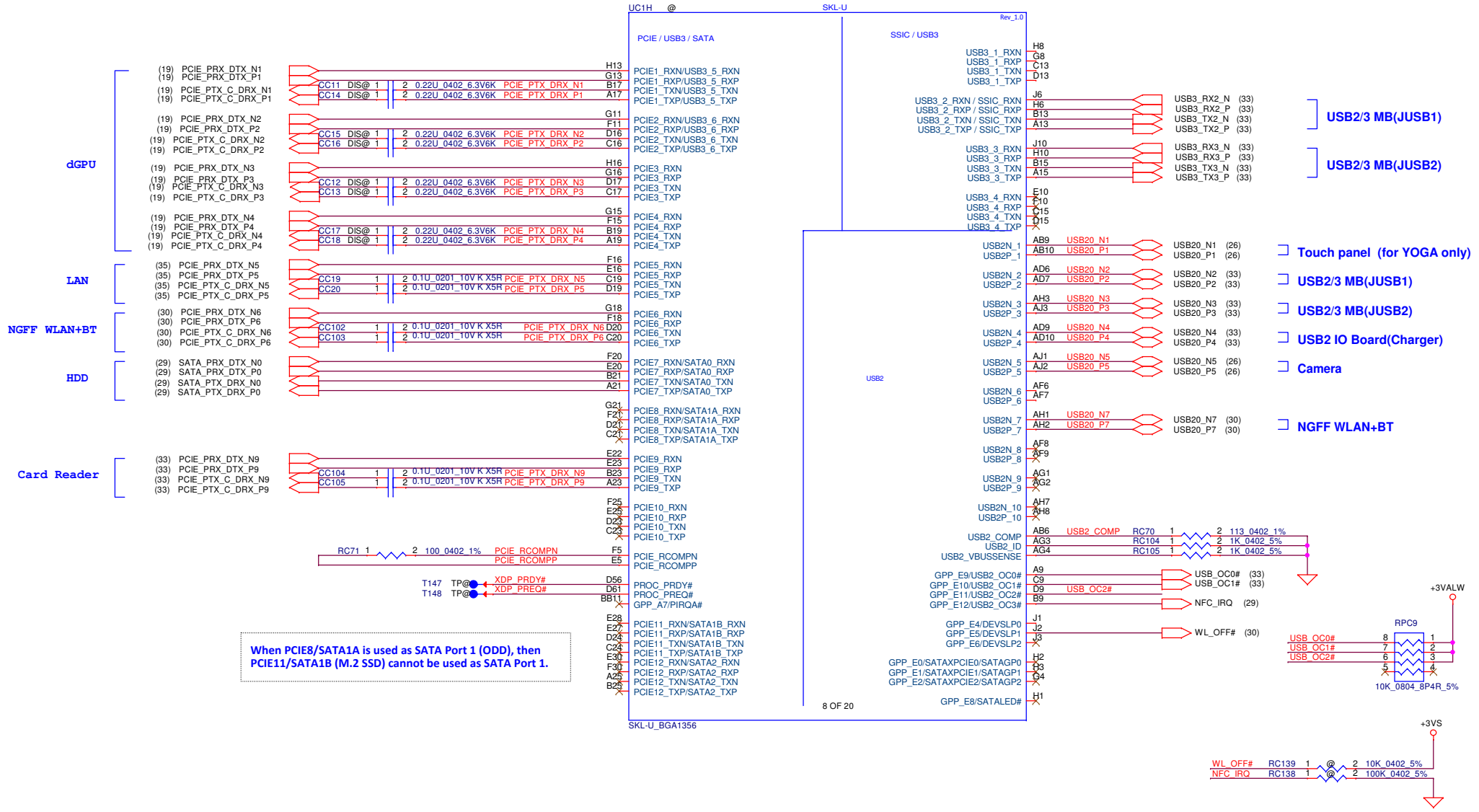


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|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |



| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title | SKL-U(7/12)PCIE,USB,SATA | | |
| Size: Custom | Document Number: LA-D451P | | Rev: 1.0 |
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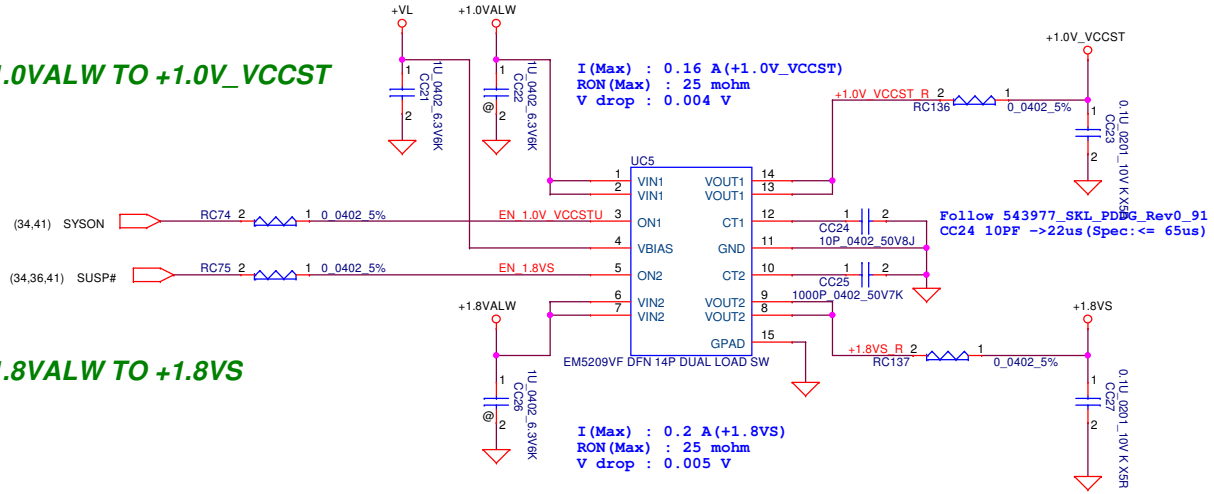
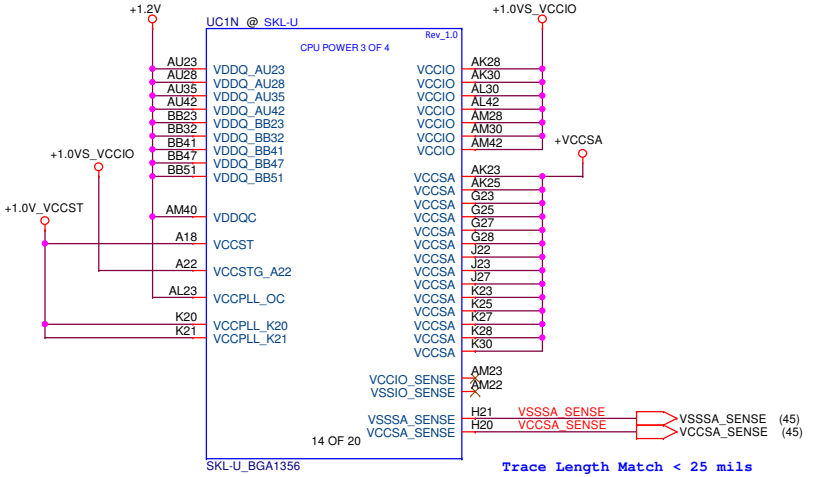
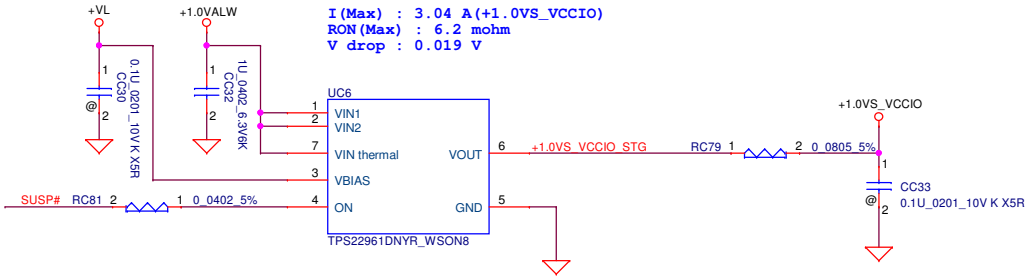
## +1.0VALW TO +1.0V_VCCST

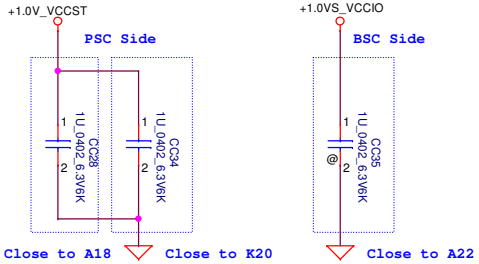



## +1.8VALW TO +1.8VS




## +1.0VALW TO +1.0VS_VCCIO

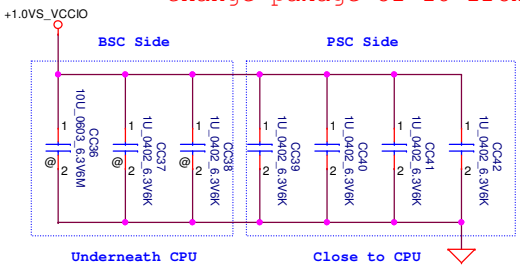


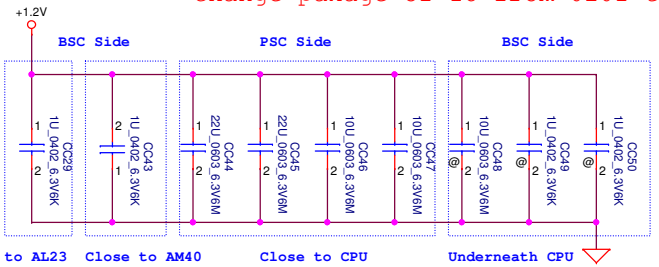




change pakage of 1U from 0201 to 0402

change pakage of 1U from 0201 to 0402

change pakage of 10U from 0402 to 0603




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |

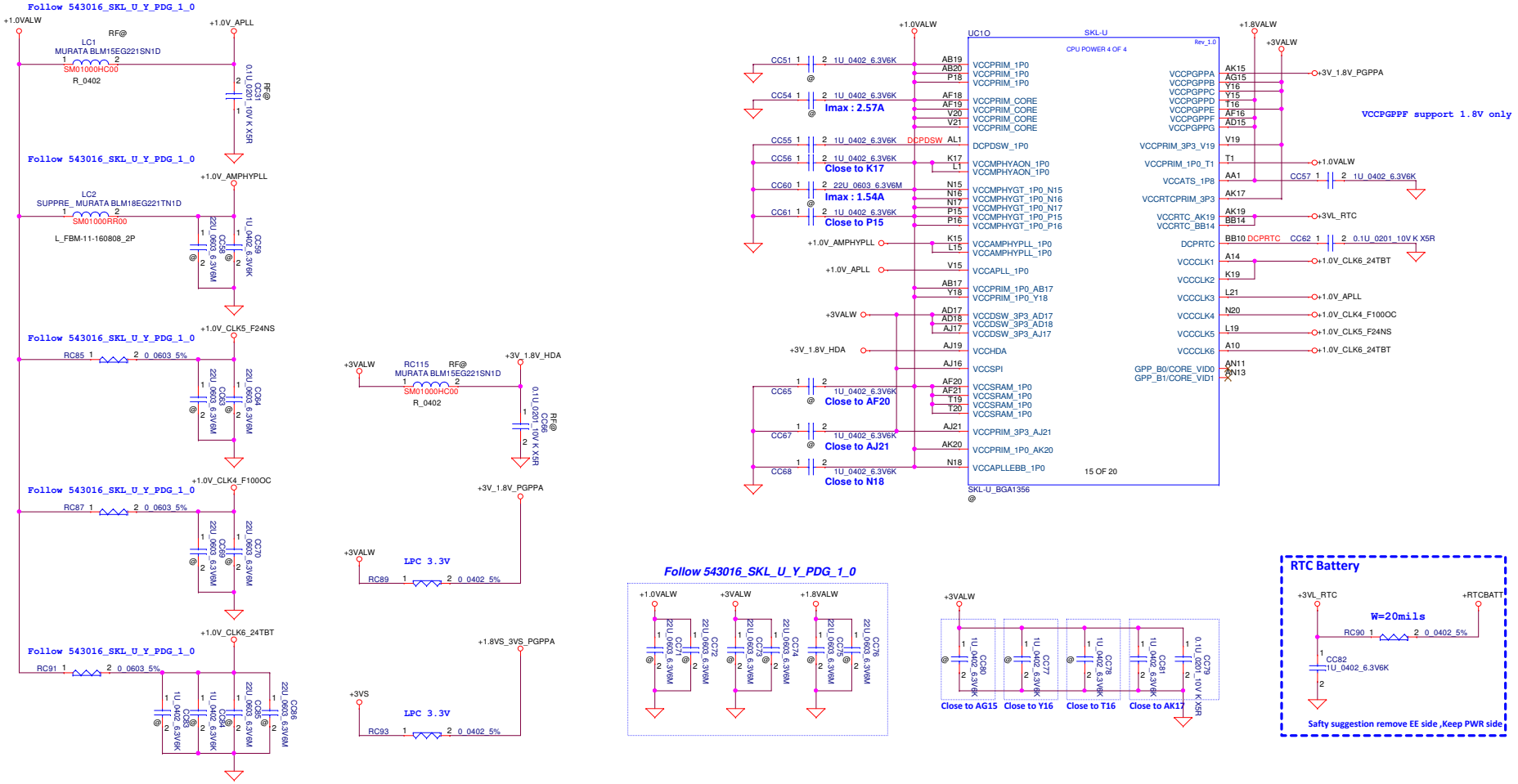


Compal Electronics, Inc.

Title: SKL-U(8/12)Power

Size: Custom | Document Number: LA-D451P | Rev: 1.0

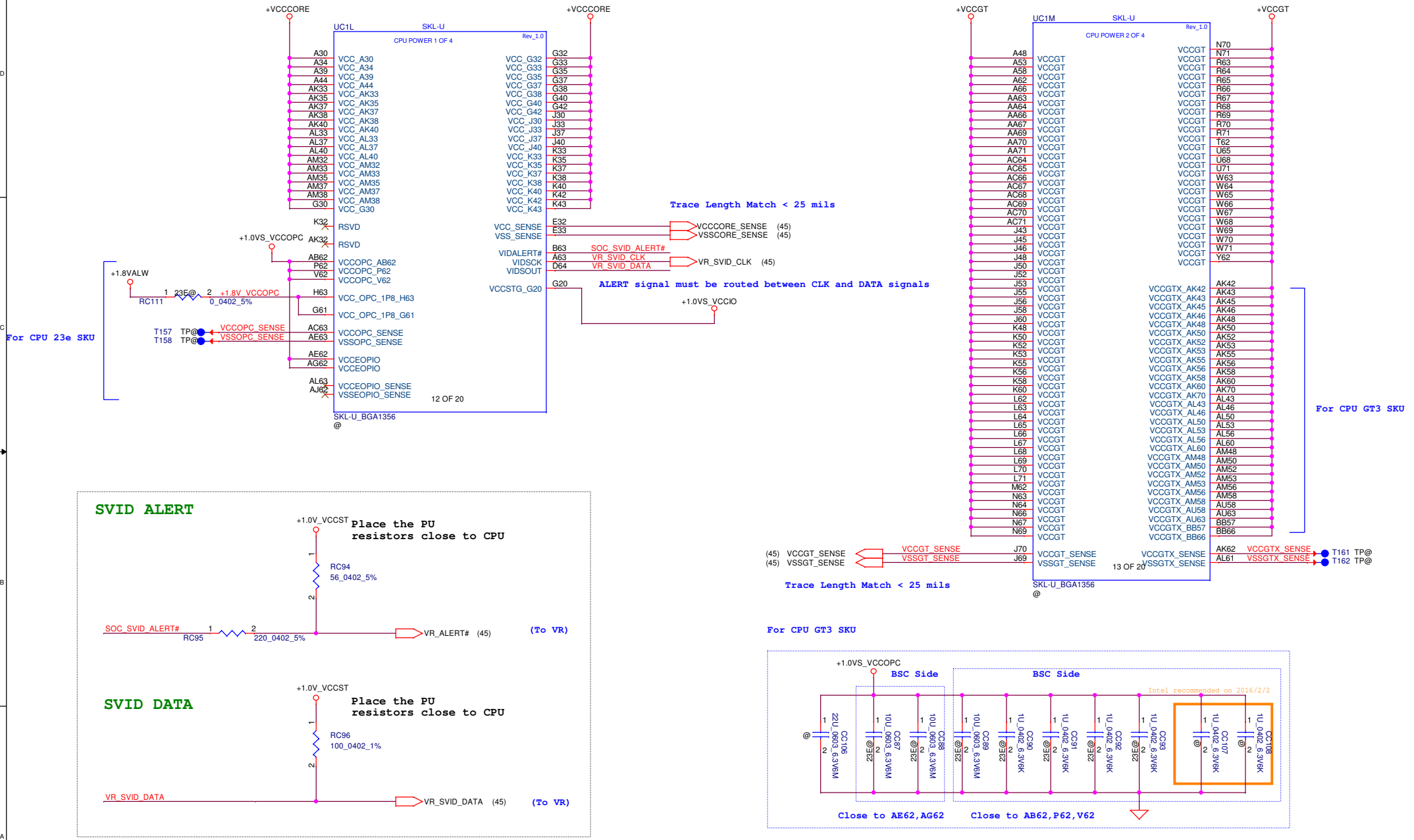
Date: Tuesday, February 16, 2016 | Sheet 13 of 50




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |



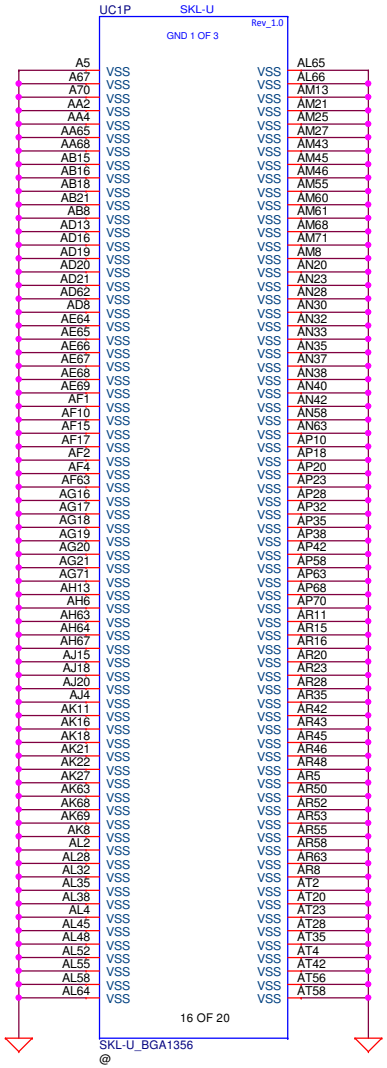
| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title | SKL-U(9/12)Power | | |
| Size: Custom | Document Number: LA-D451P | | Rev: 1.0 |
| Date: Tuesday, February 16, 2016 | Sheet 14 of 50 | | |

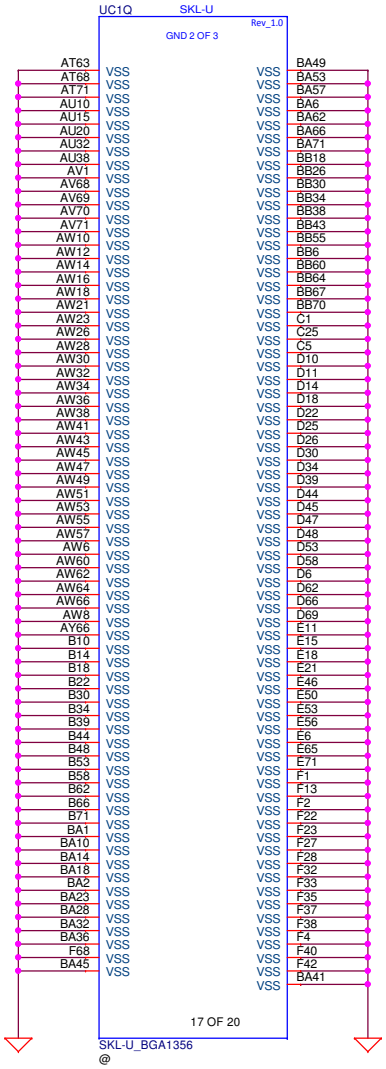


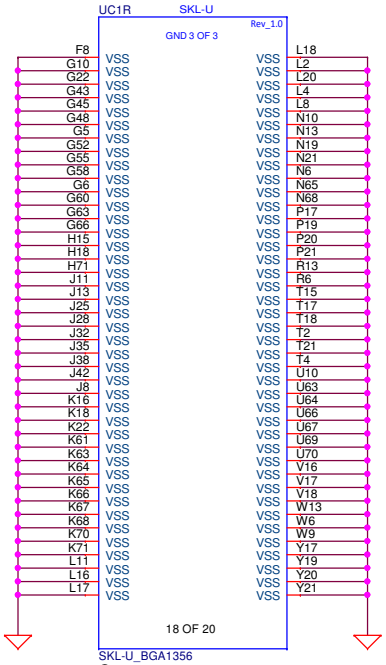

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |



| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title: SKL-U(10/12)Power,SVID | | | |
| Size: Custom | Document Number: LA-D451P | | Rev: 1.0 |
| Date: Tuesday, February 16, 2016 | Sheet 15 of 50 | | |




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |

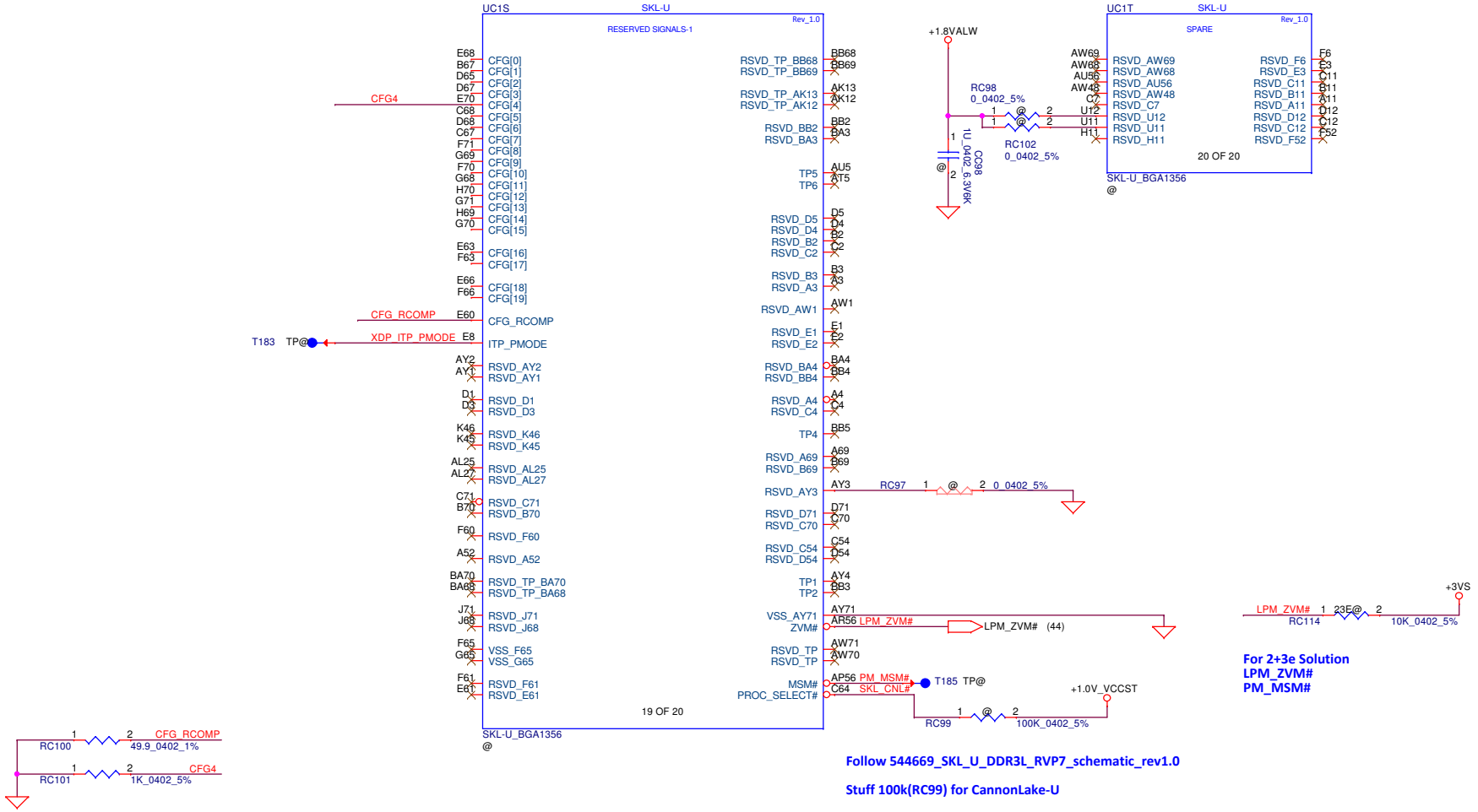


Compal Electronics, Inc.

Title: SKL-U(11/12)GND

| Size | Document Number | Rev |
|---|---|---|
| Custom | LA-D451P | 1.0 |

Date: Tuesday, February 16, 2016 Sheet 16 of 50




| Display Port Presence Strap | |
|---|---|
| CFG4 | 1 : Disabled;<br>No Physical Display Port attached to Embedded Display Port<br><br>0 : Enabled;<br>An external Display Port device is connected to the Embedded Display Port |



| Compal Electronics, Inc. | | |
|---|---|---|
| Title: SKL-U(12/12)CFG,RSVD | | |
| Size: Custom | Document Number: LA-D451P | Rev: 1.0 |
| Date: Tuesday, February 16, 2016 | Sheet 17 of 50 | |

# Reverse Type

2-3A to 1 DIMMs/channel

(7) DDR_A_DQS#[0..7]
(7) DDR_A_D[0..63]
(7) DDR_A_DQS[0..7]

(7) DDR_A_MA[0..16]
(7) DDR_A_BA0
(7) DDR_A_BA1
(7) DDR_A_BG0
(7) DDR_A_BG1

(7) DDR_A_CLK0
(7) DDR_A_CLK#0
(7) DDR_A_CLK1
(7) DDR_A_CLK#1

(7) DDR_A_CKE0
(7) DDR_A_CKE1

(7) DDR_A_CS0#
(7) DDR_A_CS1#

(8,32) PCH_SMB_DATA
(8,32) PCH_SMB_CLK

(7) DDR_A_ODT0
(7) DDR_A_ODT1

**Layout Note:**
**Place near JDIMM1**

**Note:**
**Check voltage tolerance of VREF_DQ at the DIMM socket**

4 as near side of the DIMM close to VDD pins

Place these caps on the VTT plane close to DIMM

close to DIMM

JDIMM1

DEREN_40-42271-26001RHF
LTCX006KS00
ME@

6/16 INTEL suggest

(7) DDR_A_PARITY

DDR_DRAMRST# R
DDR_DRAMRST# (7)

(7) +0.6V_VREFCA
(7) +0.6V_A_VREFDQ
+0.6V_VREFCA R
20mil
+DIMM_VREF_DQ

M_A_ACT# (7)
DDR_A_ALERT# (7)

+1.2V
+3VS
+2.5V
+0.6VS

Interleaved Memory

| Security Classification | Compal Secret Data | | |
|---|---|---|---|
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |

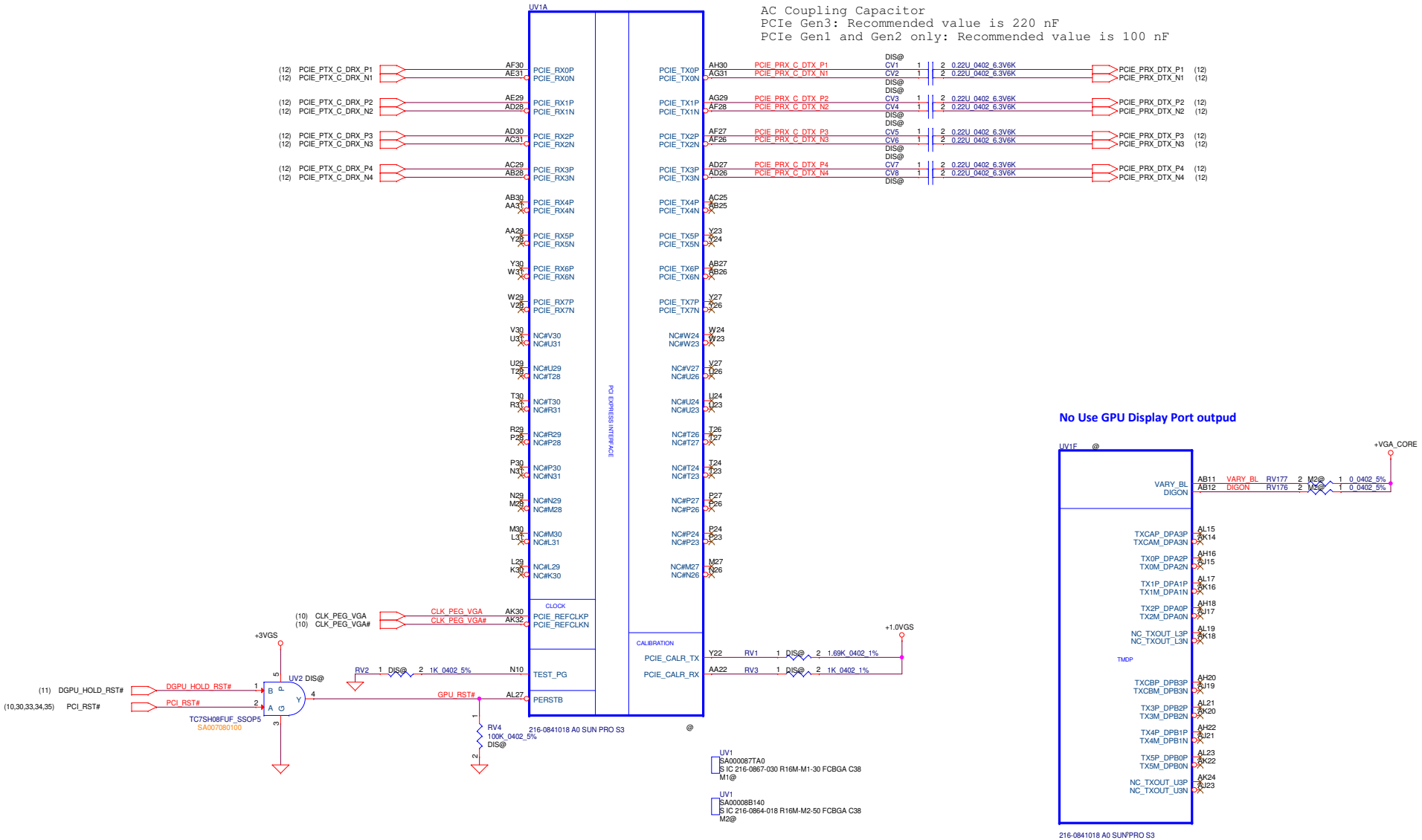


Compal Electronics, Inc.

Title: DDR4 DIMM

Size: Custom | Document Number: LA-D451P | Rev: 1.0

Date: Tuesday, February 16, 2016 | Sheet 18 of 50




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |



| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title | EXO/MESO(1/5)_PCIE/DP | | |
| Size | Document Number | | Rev |
| Custom | LA-D451P | | 1.0 |
| Date: | Tuesday, February 16, 2016 | Sheet | 19 of 50 |

**Meso/M16M-R16M-M2-50**

| |
|---|
| GPIO_11, 12, and 13 are added back.<br>The following balls cease to work as GPIOs or designated functional pins, and become **VDDC**:<br>• GPIO_1<br>• GPIO_2<br>• GPIO_14_HPD2<br>• GPIO_18_HPD3<br>The following ball ceases to work as a GPIO or designated functional pin, and becomes **NC**:<br>• GPIO_7_BLON |
| "Topaz" allocates 11 more VDDC balls so that the total number of VDDC balls becomes 36.<br>The following functional balls on earlier generations of ASICs are reassigned as the additional VDDC balls:<br>• VARY_BL (AB11)<br>• DIGON (AB12)<br>• GENERCA (AB13)<br>• GENERICC (W9)<br>• DDC2CLK (AC11)<br>• DDC2DATA (AC13)<br>• HPD1 (AC14)<br>• GPIO_1 (U10)<br>• GPIO_2 (T10)<br>• GPIO_18 (W10)<br>• GPIO_14_HPD2 (Y9) |

**Exo/R16M-M1-30**

| |
|---|
| The following balls cease to work as GPIOs or designated functional pins, and become **NC**:<br>• GPIO_1<br>• GPIO_2<br>• GPIO_7_BLON<br>• GPIO_11<br>• GPIO_12<br>• GPIO_13<br>• GPIO_14_HPD2<br>• GPIO_18_HPD3 |
| "Jet"/"Sun" has a total of 25 VDDC balls.<br>The 11 balls listed in the "Topaz" column are NC on "Jet"/"Sun". |

**Resistor Divider Lookup Lable**

| R_pu (ohm) | R_pd (ohm) | Bitd [3:1] |
|---|---|---|
| NC | 4.75k | 000 |
| 8.45k | 2k | 001 |
| 4.53k | 2k | 010 |
| 6.98k | 4.99k | 011 |
| 4.53k | 4.99k | 100 |
| 3.24k | 5.62k | 101 |
| 3.4k | 10k | 110 |
| 4.75k | NC | 111 |

0402 1% resistors are equired

**Capacitor Divider Lookup Lable**

| Cap (nF) | Bitd [5:4] |
|---|---|
| 680nF | 00 |
| 82nF | 01 |
| 10nF | 10 |
| NC | 11 |

PS_0[3:1]=001
PS_0[5:4]=11

Strap Name :
- PS_0[1] ROM_CONFIG[0]
- PS_0[2] ROM_CONFIG[1]
- PS_0[3] ROM_CONFIG[2]
- PS_0[4] N/A
- PS_0[5] AUD_PORT_CONN_PINSTRAP[0]

PS_1[3:1]=001
PS_1[5:4]=11

Strap Name :
- PS_1[1] STRAP_BIF_GEN3_EN_A
- PS_1[2] TRAP_BIF_CLK_PM_EN
- PS_1[3] N/A
- PS_1[4] STRAP_TX_CFG_DRV_FULL_SWING
- PS_1[5] STRAP_TX_DEEMPH_EN

PS_2[3:1]=000
PS_2[5:4]=11
AMD recommend 09/25

Strap Name :
- PS_2[1] N/A
- PS_2[2] N/A
- PS_2[3] STRAP_BIOS_ROM_EN
- PS_2[4] STRAP_BIF_VGA_DIS
- PS_2[5] N/A

PS_3[3:1]=000
PS_3[5:4]=11

Strap Name :
- PS_3[1] BOARD_CONFIG[0] (Memory ID)
- PS_3[2] BOARD_CONFIG[1] (Memory ID)
- PS_3[3] BOARD_CONFIG[2] (Memory ID)
- PS_3[4] AUD_PORT_CONN_PINSTRAP[1]
- PS_3[5] AUD_PORT_CONN_PINSTRAP[2]

**MLPS Memory ID setting:**

| BOARD_CONFIG[2:0] | | Memory Type | Configuration | Channel Size | Vendor P/N | SMT quantity |
|---|---|---|---|---|---|---|
| ID | [2:0] | | | | | |
| 0 | 000 | Samsung-DDR3 | 256M x 16 4PCS, 1 Rank | 2GB | K4W4G1646E-BC1A | 4 pcs |
| 1 | 001 | Hynix-DDR3 | 256M x 16 4PCS, 1 Rank | 2GB | H5TC4G63CFR-N0C | 4 pcs |
| 2 | 010 | Micron-DDR3 | 256M x 16 4PCS, 1 Rank | 2GB | MT41J256M16LY-091G:N | 4 pcs |

ZZZ2 Hynix 2G H2G@ Part Number = X7666638L01
ZZZ3 Samsung 2G S2G@ Part Number = X7666638L02
ZZZ1 Micron 2G M2G@ Part Number = X7666638L03

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |



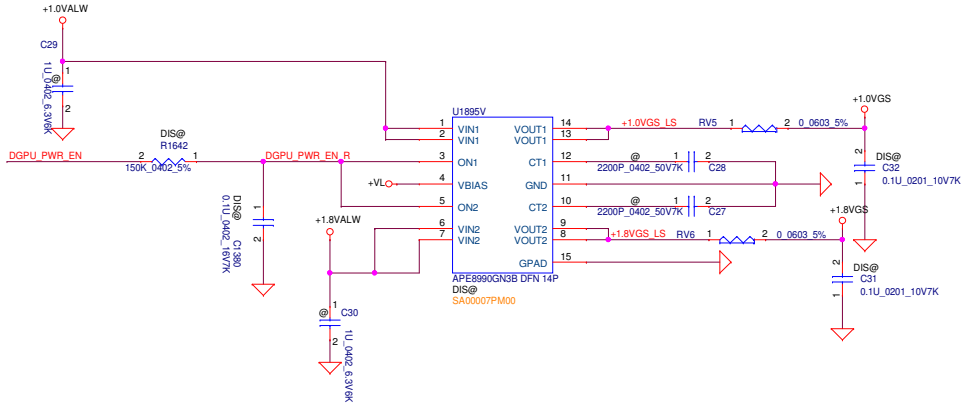
Compal Electronics, Inc.

Title: EXO/MESO(2/5)_MSIC

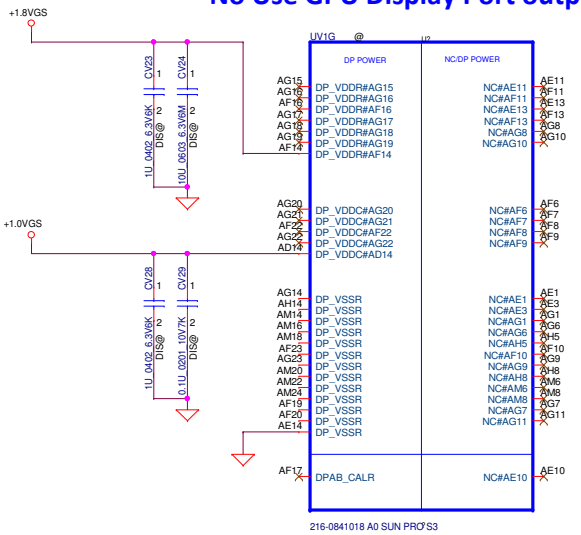
Size: Custom | Document Number: LA-D451P | Rev: 1.0

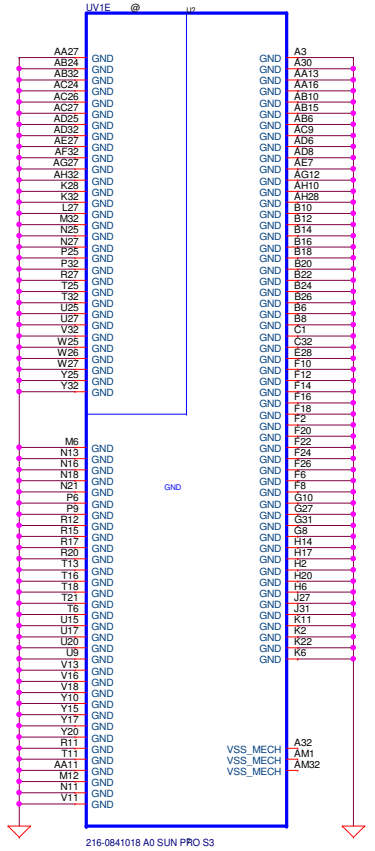
Date: Tuesday, February 16, 2016 | Sheet 20 of 50

## +1.8VALW TO +1.8VGS
## +1.0VALW TO +1.0VGS
## Load switch

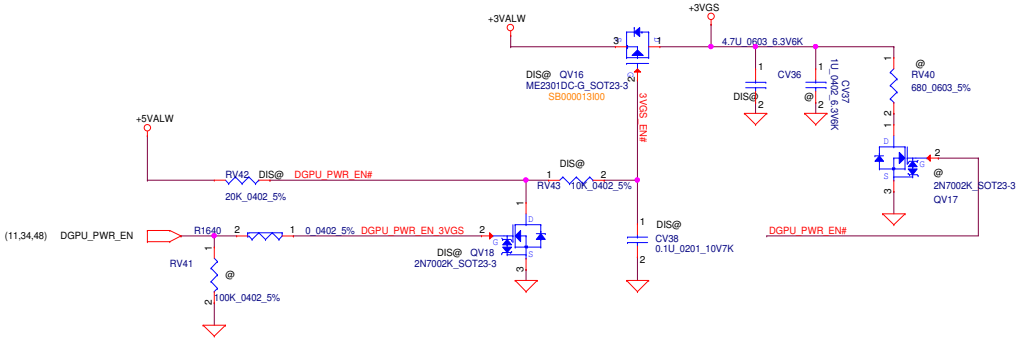


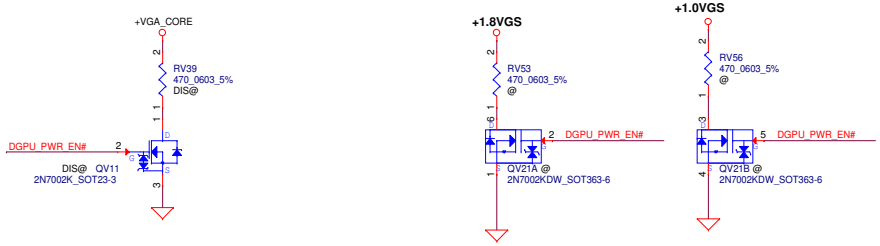

## No Use GPU Display Port outpud




## +3VS to +3VGS




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |

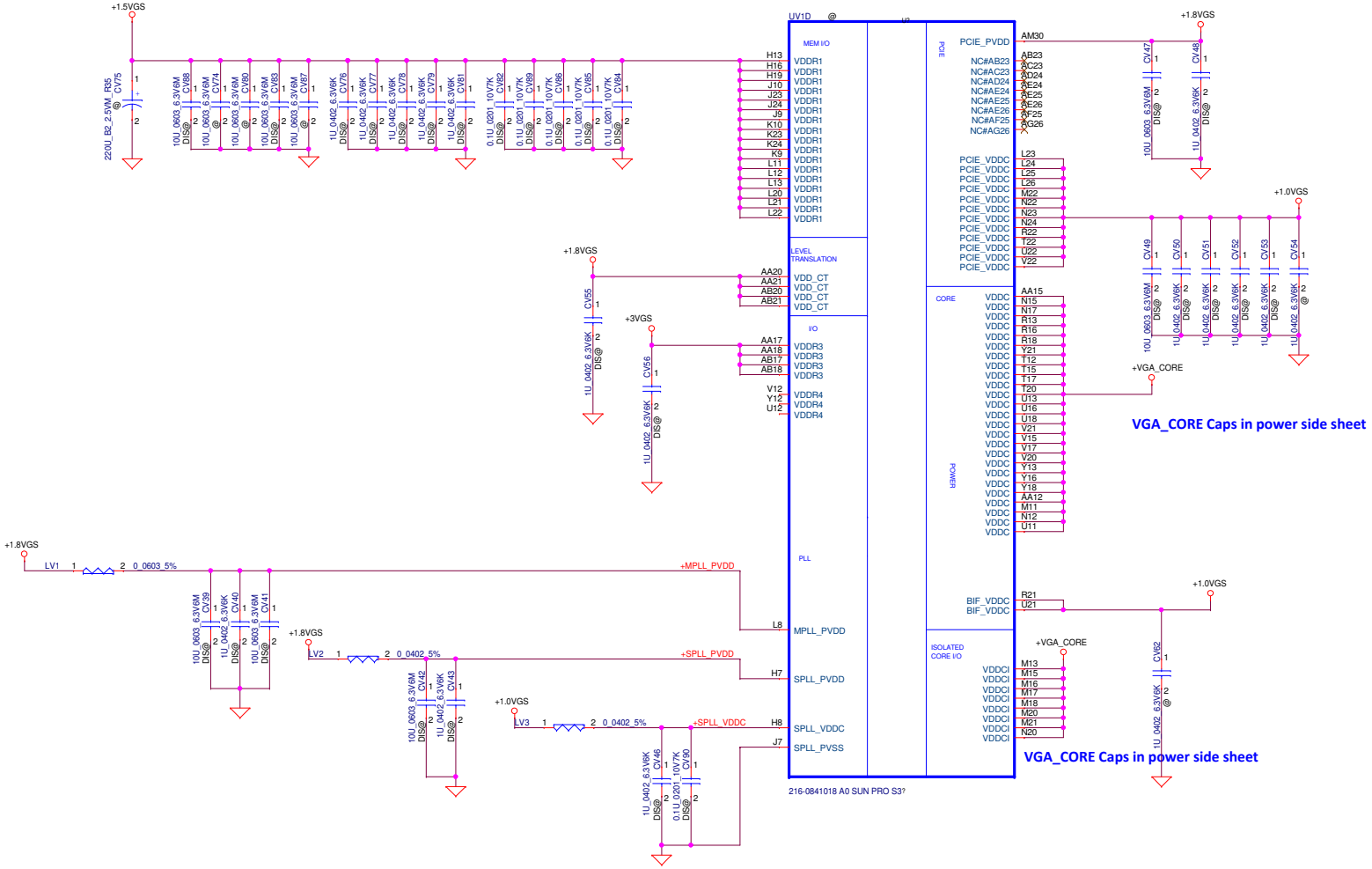


Compal Electronics, Inc.

Title: EXO/MESO(3/5)_PWR/GND

Size: Custom | Document Number: LA-D451P | Rev: 1.0

Date: Tuesday, February 16, 2016 | Sheet 21 of 50




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |



Compal Electronics, Inc.

Title: EXO/MESO(4/5)_PWR

| Size | Document Number | Rev |
|---|---|---|
| Custom | LA-D451P | 1.0 |

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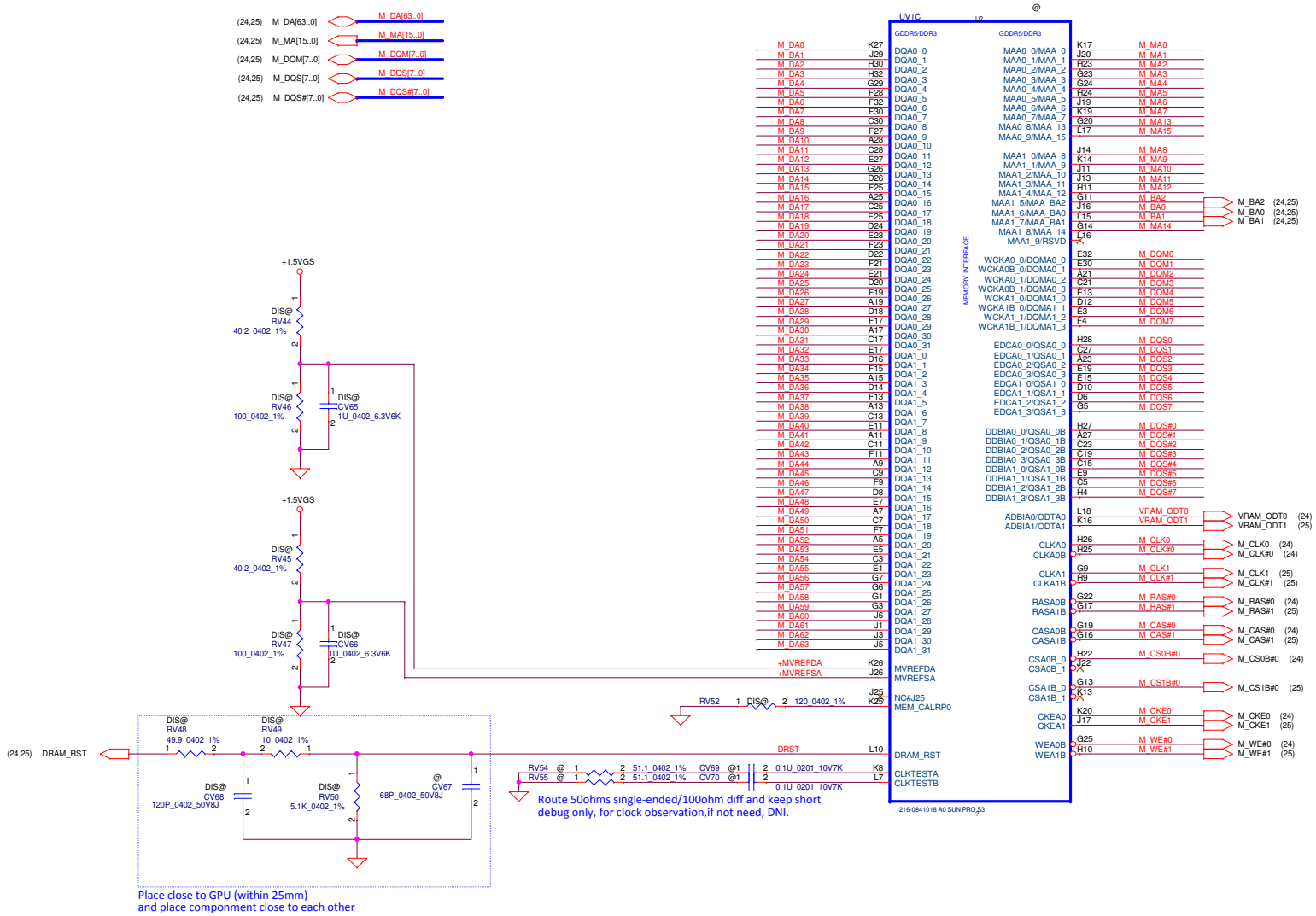



| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |



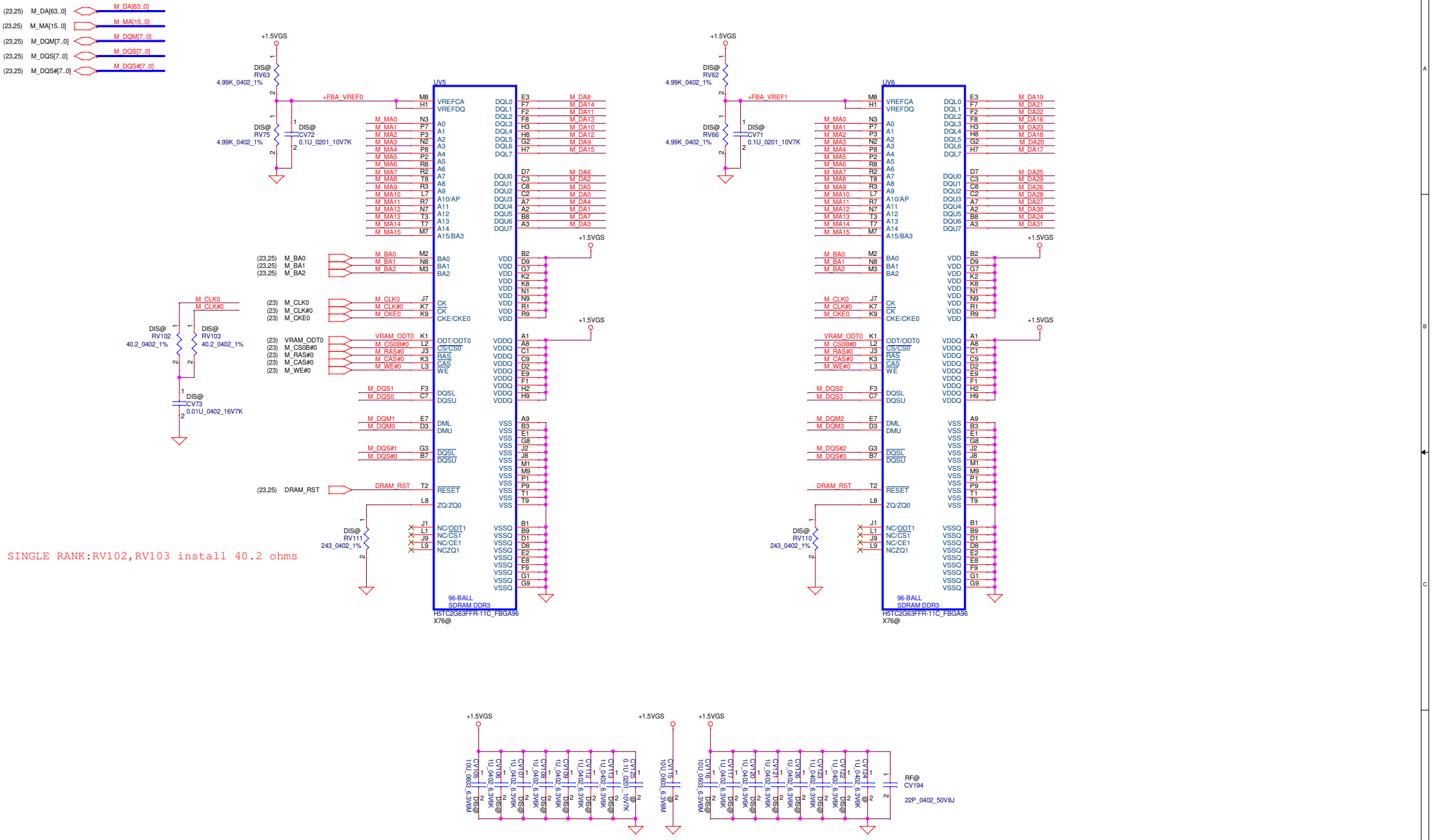
Compal Electronics, Inc.

Title: EXO/MESO(5/5)_MEM

| Size | Document Number | Rev |
|---|---|---|
| Custom | LA-D451P | 1.0 |

Date: Tuesday, February 16, 2016 Sheet 23 of 50

# DDR3 Memory Channel Rank 0:A0




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |



Compal Electronics, Inc.

Title: EXO/MESO_DDR3L_A1 Rank 0

| Size | Document Number | Rev |
|---|---|---|
| Custom | LA-D451P | 1.0 |

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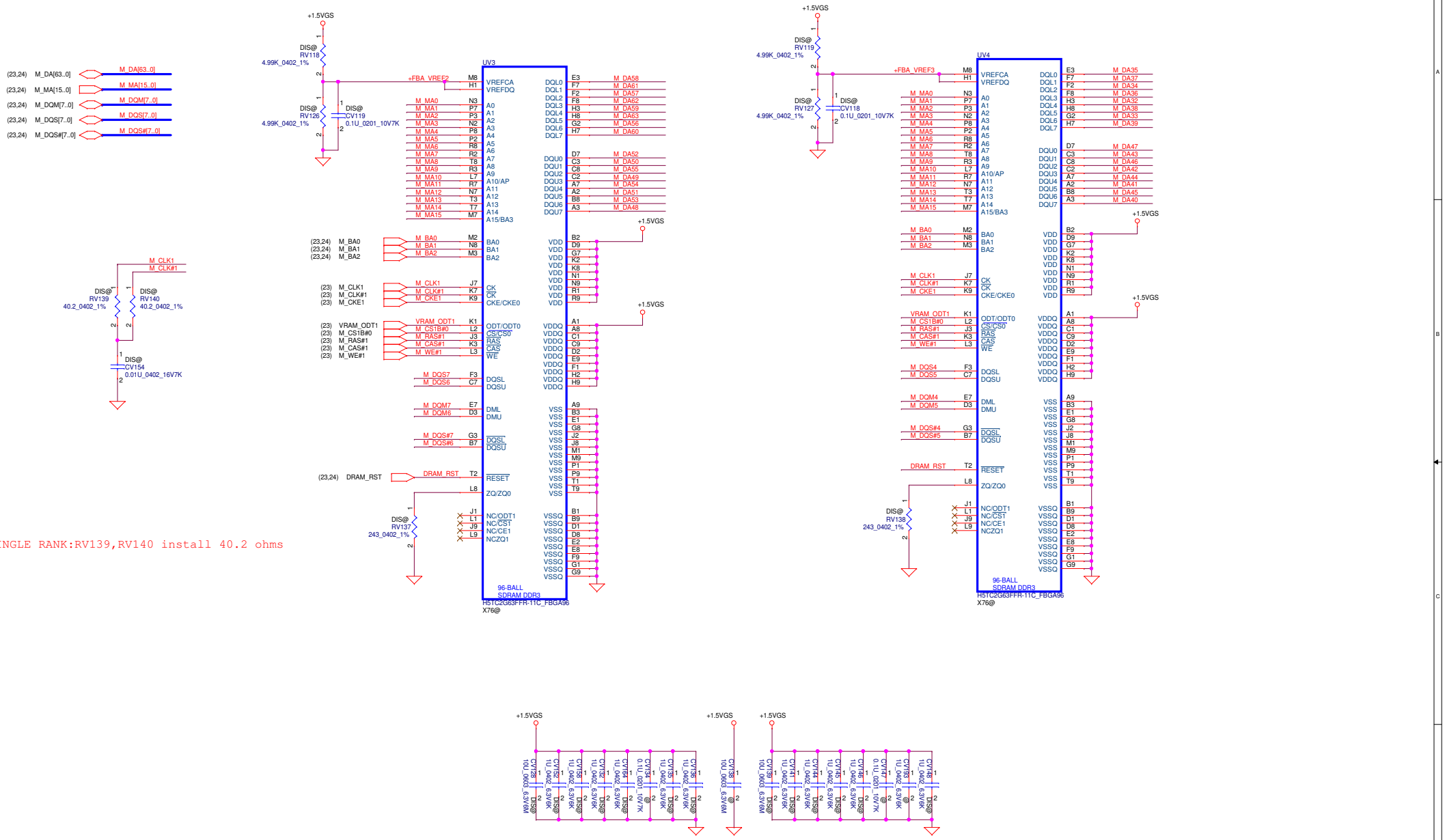
# DDR3 Memory Channel Rank 0:A1




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |



Compal Electronics, Inc.

Title: EXO/MESO_DDR3L_A2 Rank 0

| Size | Document Number | Rev |
|---|---|---|
| Custom | LA-D451P | 1.0 |

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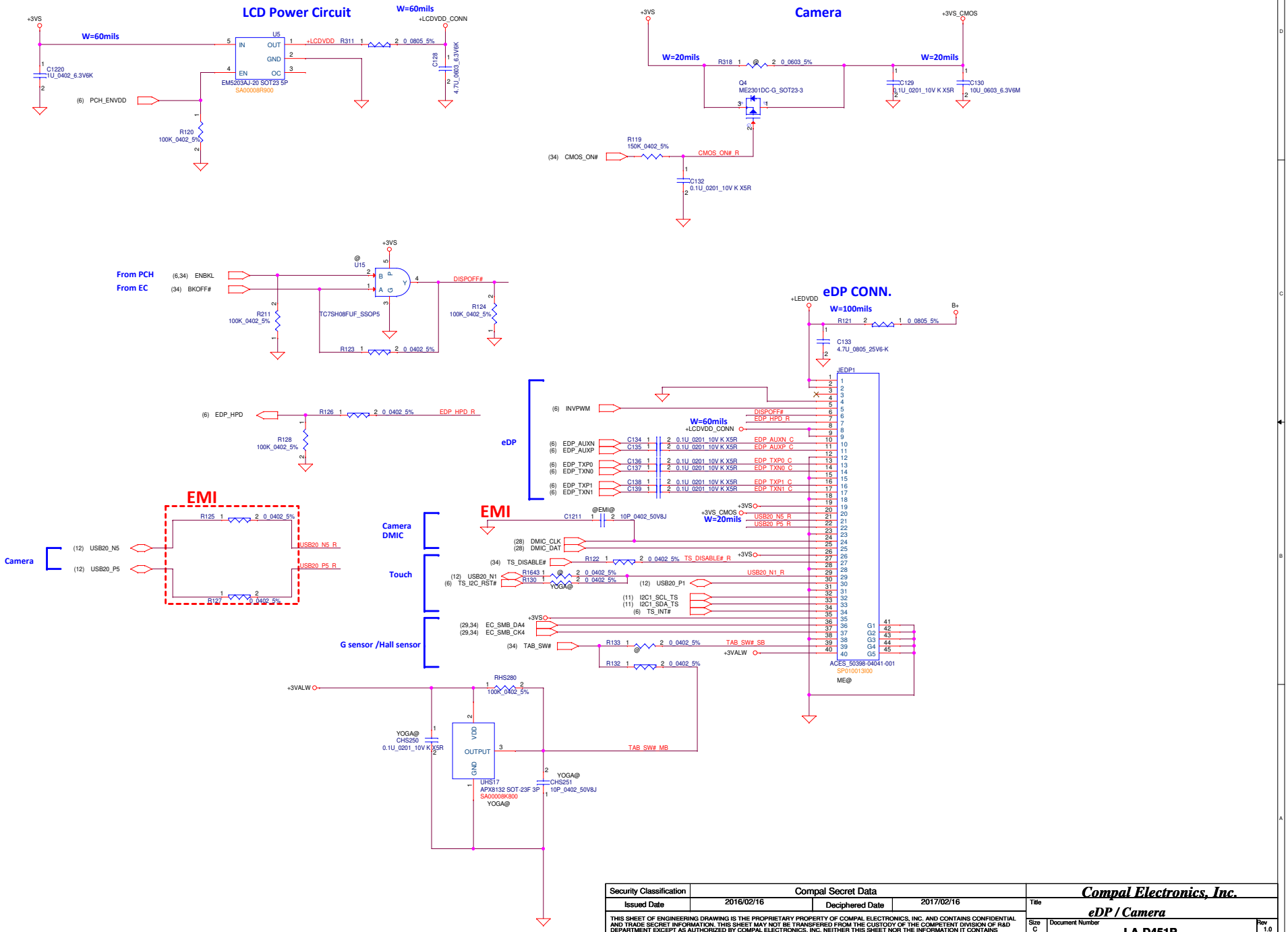



| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |



**Compal Electronics, Inc.**

Title: **eDP / Camera**

| Size | Document Number | Rev |
|---|---|---|
| C | LA-D451P | 1.0 |

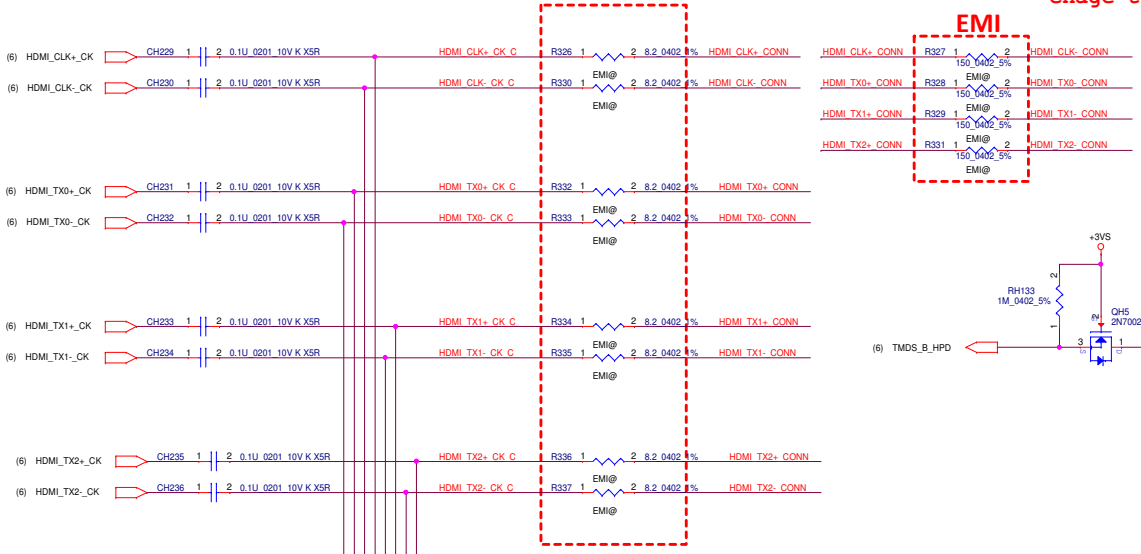
Date: Tuesday, February 16, 2016 | Sheet 26 of 50

EMI

Near JHDMI1

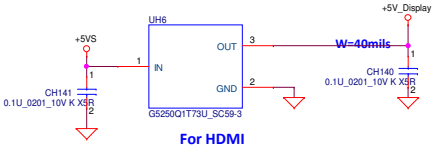
change to 8.2 from 10

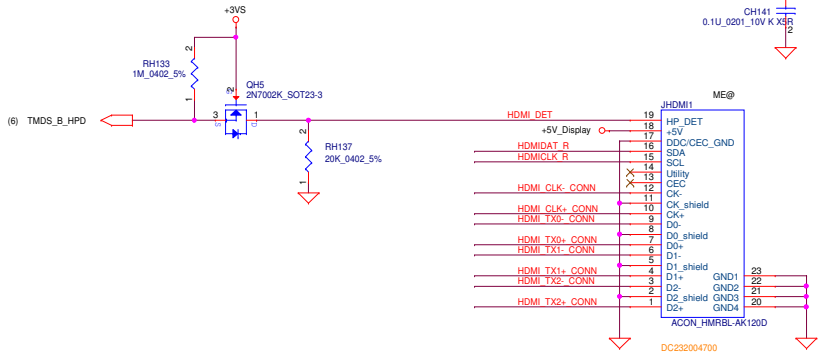
chage to EMI@ from @

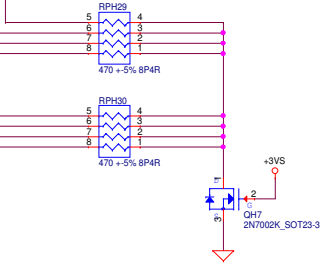


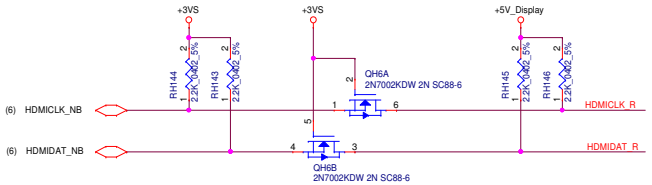

EMI

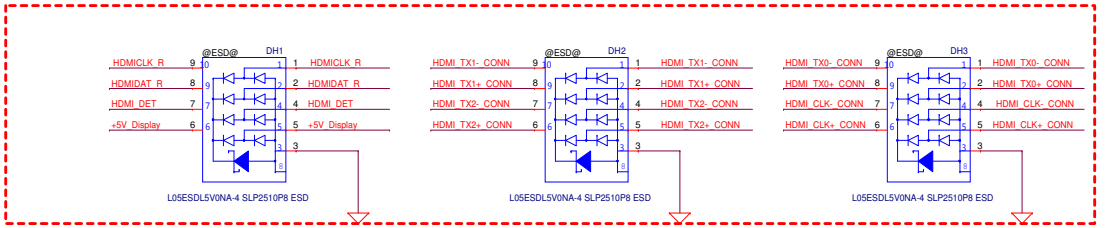


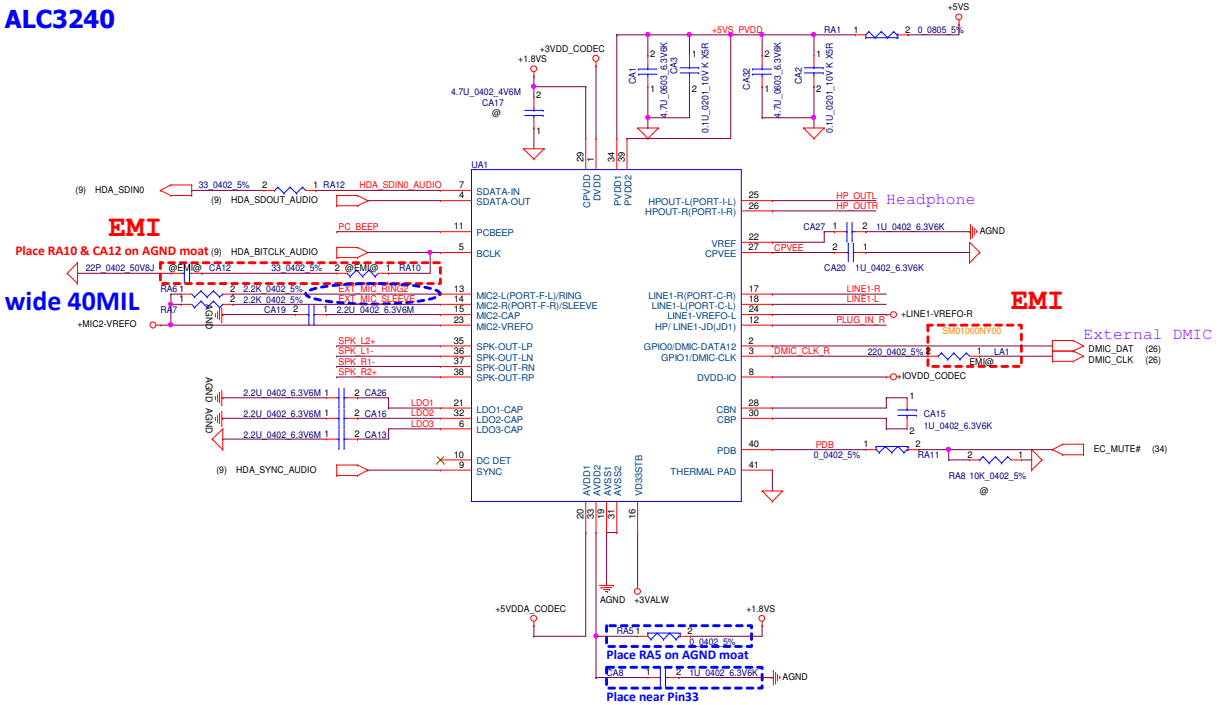




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | Compal Electronics, Inc. |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |

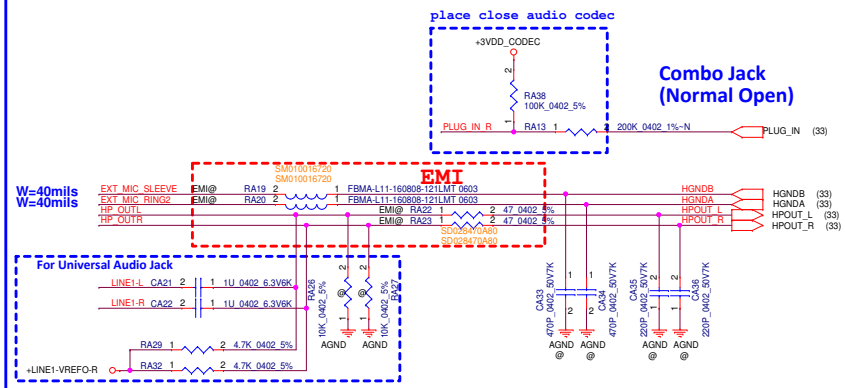


| | | | |
|---|---|---|---|
| Title | HDMI | | |
| Size C | Document Number LA-D451P | | Rev 1.0 |
| Date: Tuesday, February 16, 2016 | Sheet 27 of 50 | | |

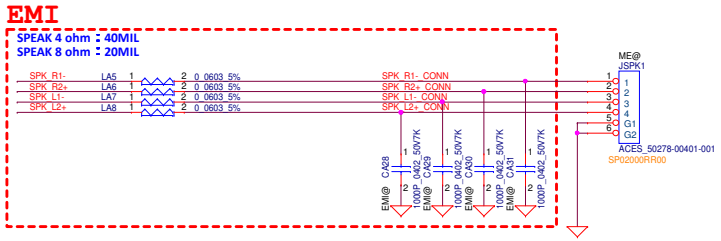
# ALC3240



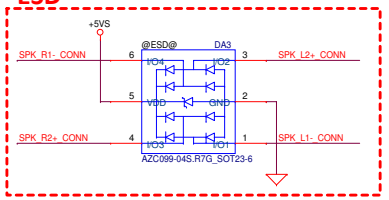

# Input



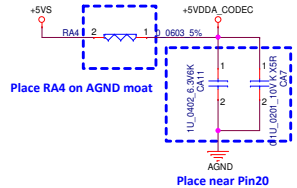

# Output




ESD protection needs to be placed near connector side




## +5VS → +5VDDA_CODEC



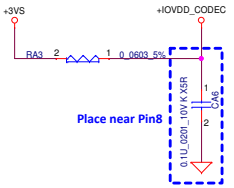

## Each Platform Power Net Support List :

| | +1.5VS | +1.8VS | +3VS | +5VS | +3VALW |
|---|---|---|---|---|---|
| | 1.5V(S0) | 1.8V(S0) | 3.3V(S0) | 5V(S0) | 3.3V(S0~S5) |
| Intel Broadwell | V | X | V | V | V |
| Intel Skylake | X | V | V | V | V |

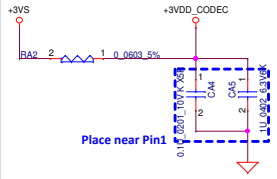
## Each Platform HDA Link Voltage Support (Pin 8) :

| | 3.3V | 1.5V |
|---|---|---|
| Intel Broadwell | V (default) | V |
| Intel Skylake | V (default) | V |

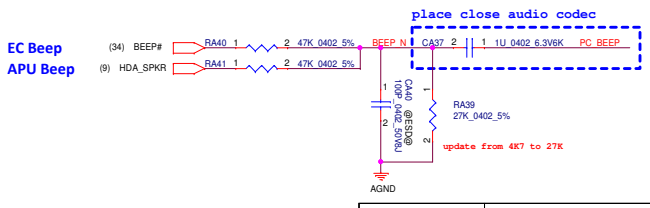
## +3VS → +IOVDD_CODEC



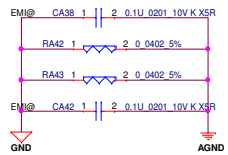

## +3VS → +3VDD_CODEC




## PC Beep

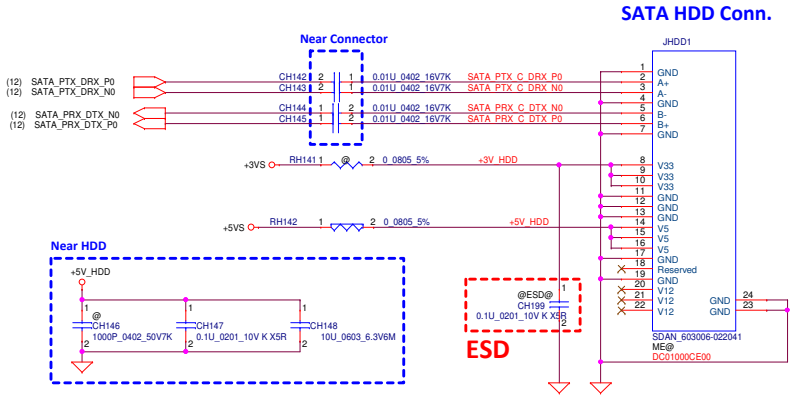



## EMI

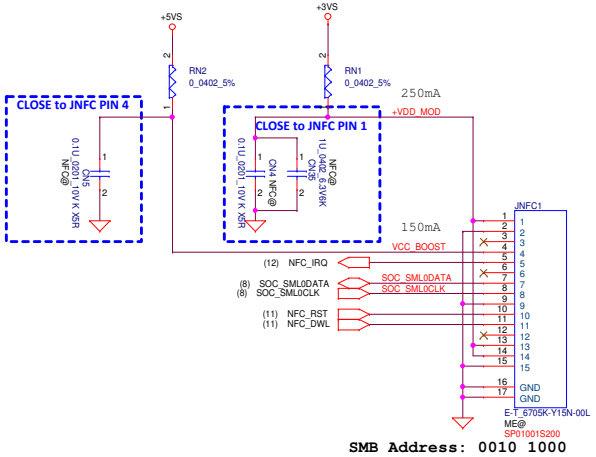



| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | Compal Electronics, Inc. |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |
| Title | HD Audio Codec_ALC3240 | | |
| Size C | Document Number LA-D451P | | Rev 1.0 |
| Date: Tuesday, February 16, 2016 | Sheet 28 of 50 | | |

# HDD

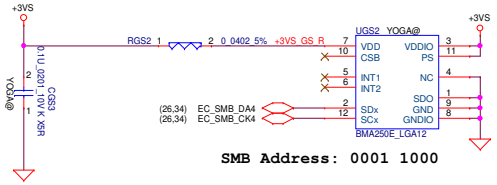



# NFC




SMB Address: 0010 1000

# (G-Sensor for 360-degree reverse)




SMB Address: 0001 1000

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |



Compal Electronics, Inc.

Title: HDD/TPM/APS/NFC

| Size | Document Number | Rev |
|---|---|---|
| C | LA-D451P | 1.0 |

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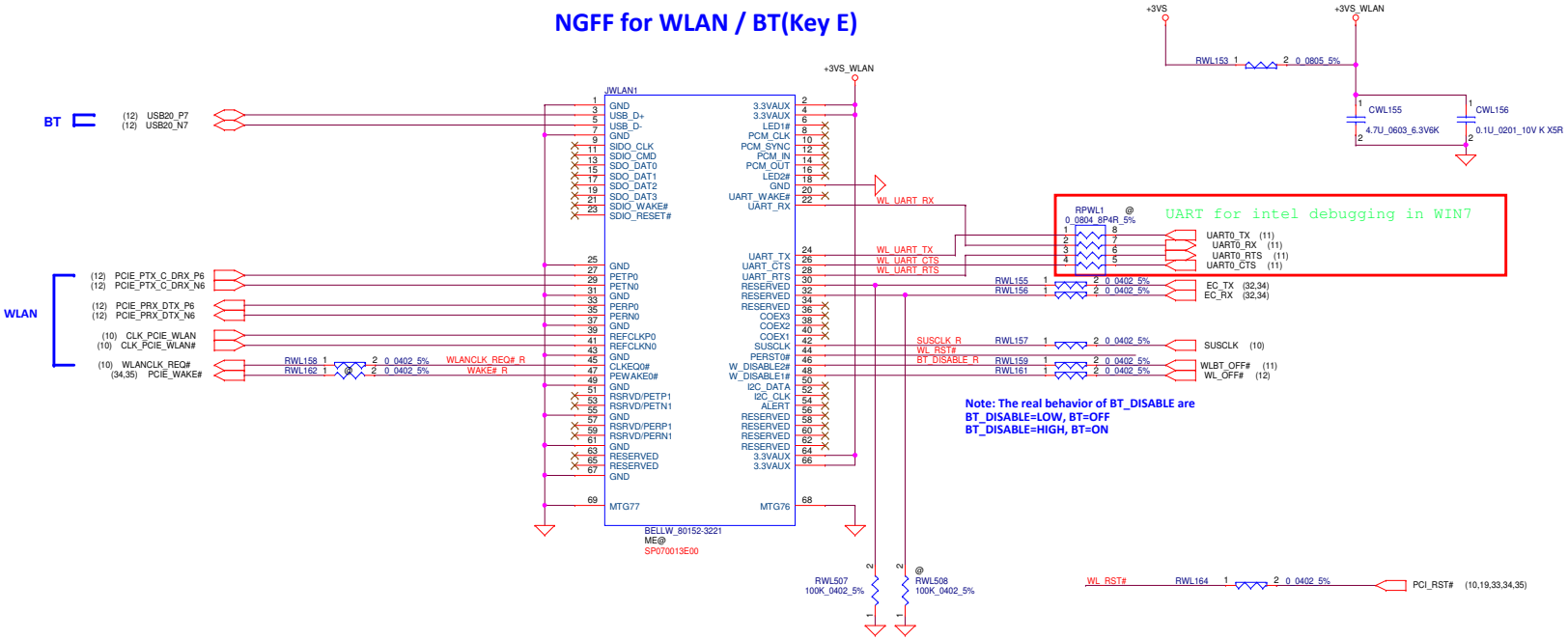
# NGFF for WLAN / BT(Key E)

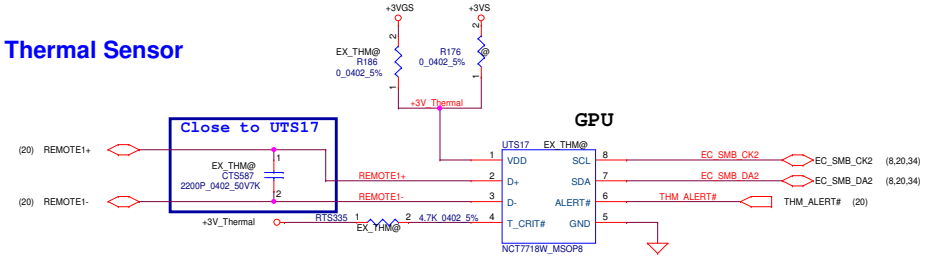



| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |



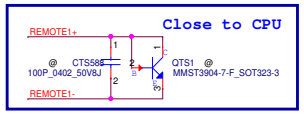
| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title: NGFF WLAN / BT | | | |
| Size | Document Number: LA-D451P | | Rev: 1.0 |
| Date: Tuesday, February 16, 2016 | | Sheet 30 of 50 | |

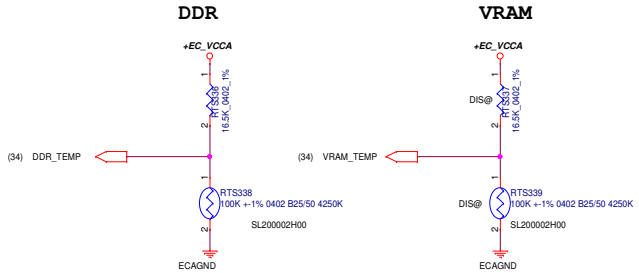
## Thermal Sensor

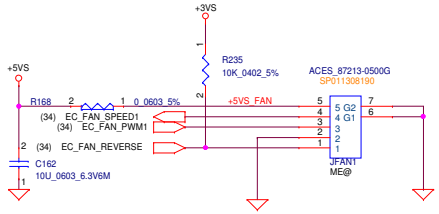


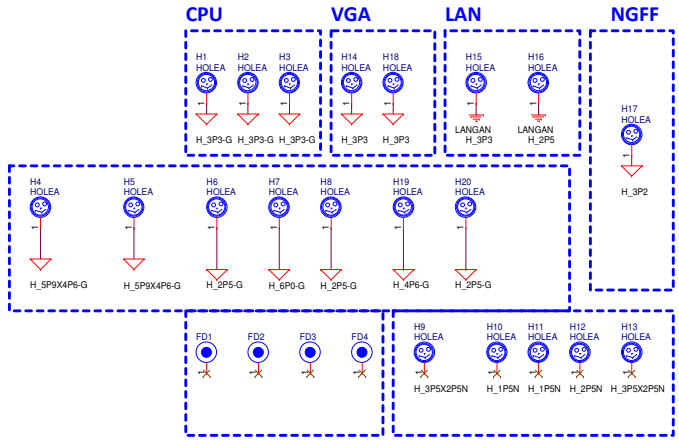

**SMB Address: 1001100x**

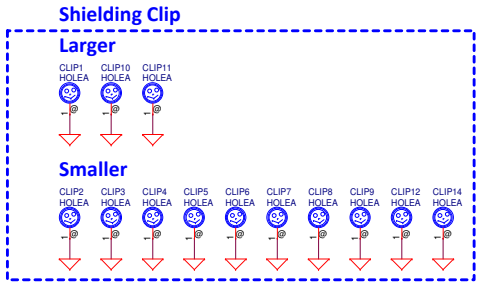
REMOTE1+/-:
Trace width/space:10/10 mil
Trace length:<8"




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |



*Compal Electronics, Inc.*

Title: **FAN / Thermal Senser**

| Size | Document Number | Rev |
|---|---|---|
| C | LA-D451P | 1.0 |

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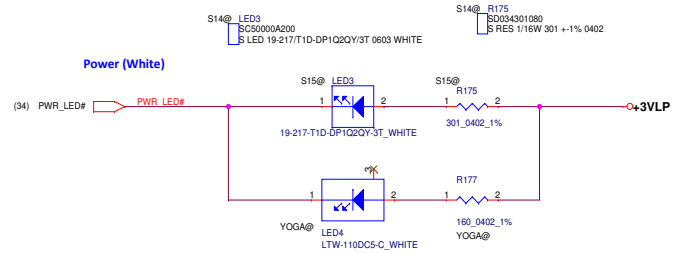
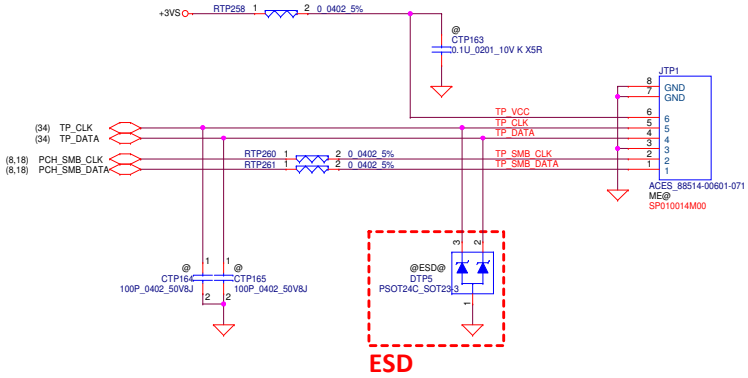
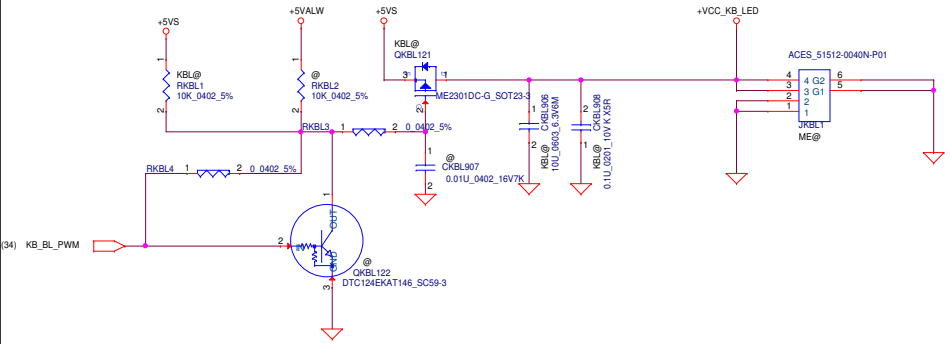
# Power Button LED



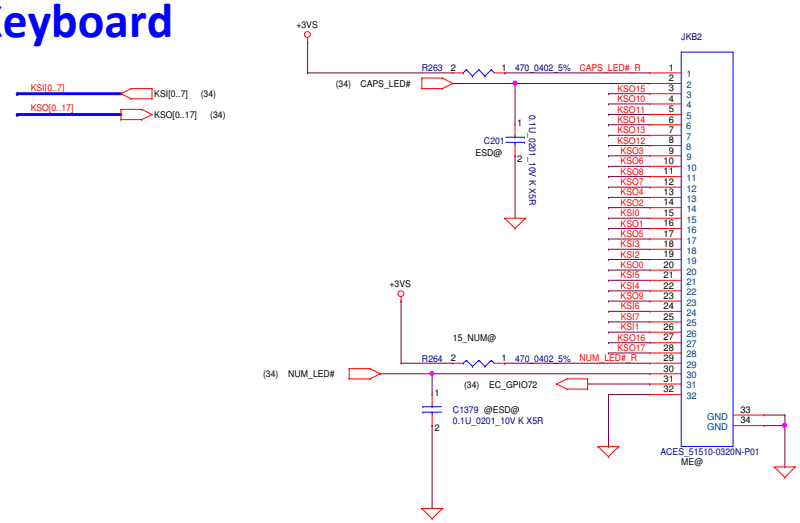

# Touch Pad



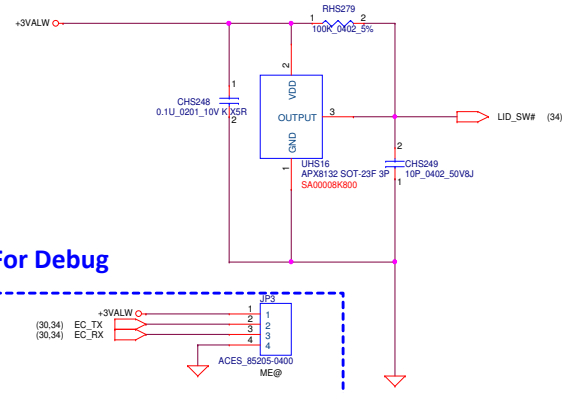

# Keyboard Backlight




# Keyboard



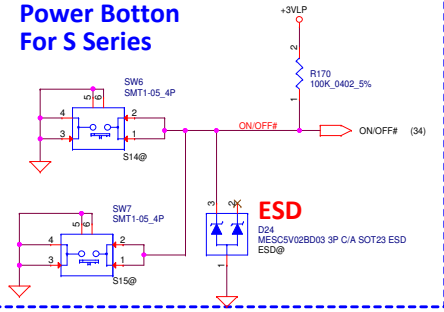

# Hall Senser & Button



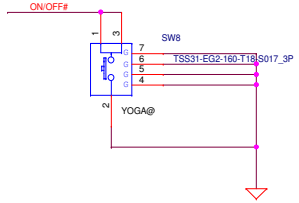

## For Debug




## Power Botton For S Series




## Power Botton For YOGA

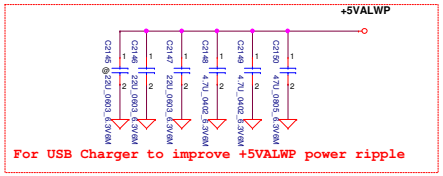


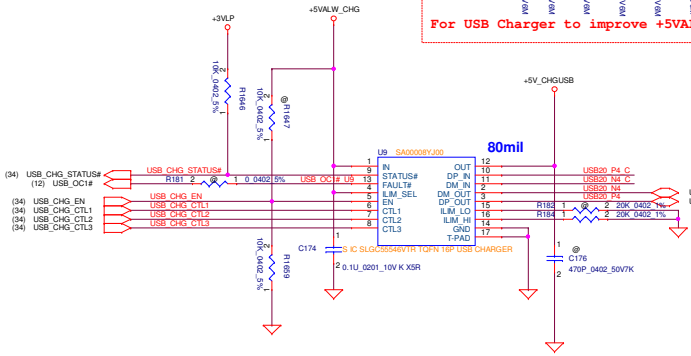

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |



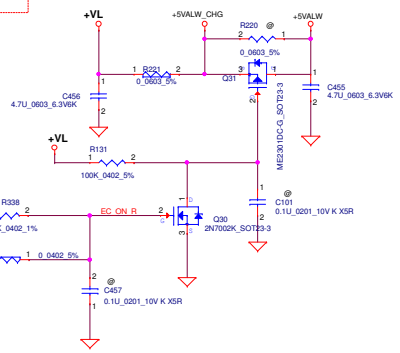
| | | | |
|---|---|---|---|
| Compal Electronics, Inc. | | | |
| Title | KBL/KBD/LED/TP/HS Conn. | | |
| Size C | Document Number LA-D451P | | Rev 1.0 |
| Date: Tuesday, February 16, 2016 | Sheet 32 of 50 | | |

# USB Charge

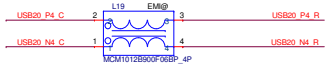


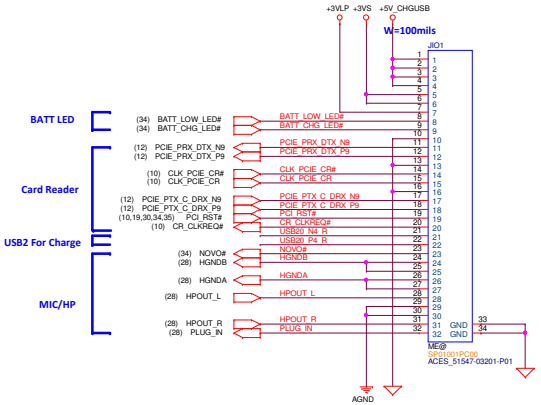

# USB Charge switch



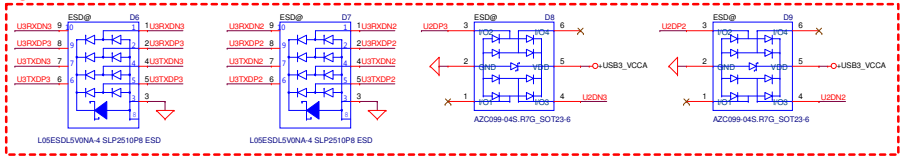

# EMI




# IO CONN



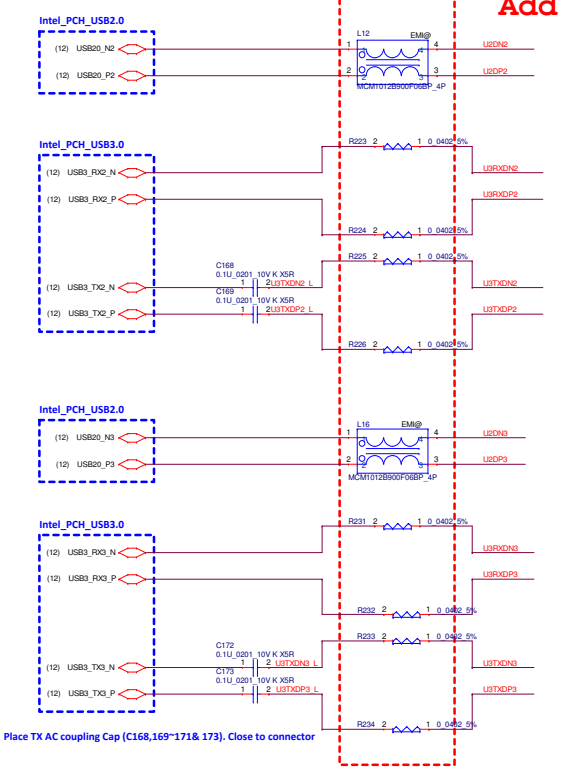

# ESD



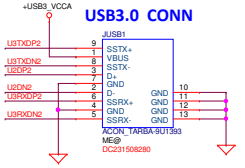

# USB3.0_Port

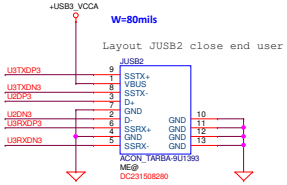
# EMI

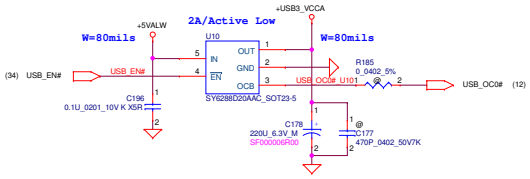
## Add resistor




Place TX AC coupling Cap (C168,169~171& 173). Close to connector



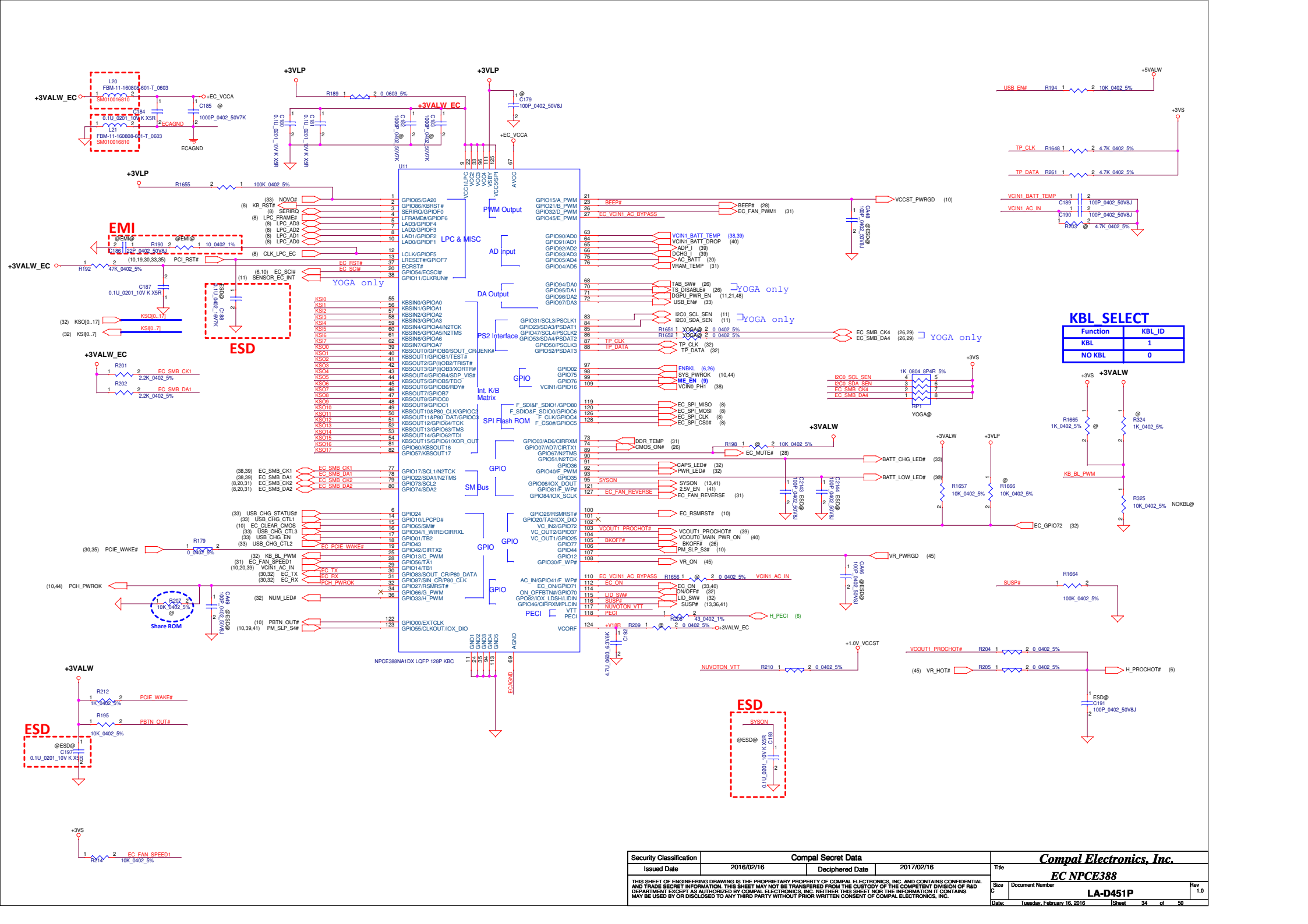



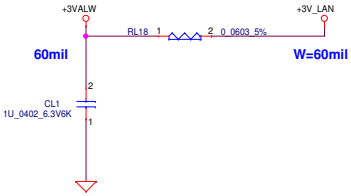



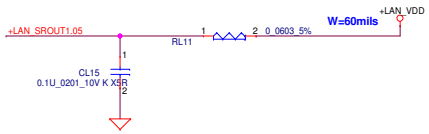

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | Compal Electronics, Inc. |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |



| | | | |
|---|---|---|---|
| Title | USB2 / USB3 / FP / IO Board | | |
| Size: Custom | Document Number: LA-D451P | | Rev: 1.0 |
| Date: Tuesday, February 16, 2016 | Sheet 33 of 50 | | |


+3VALW_EC
+3VLP
+3VS
+5VALW
+1.0V_VCCST
U11
NPCE388NA1DX LQFP 128P KBC
EMI
ESD
YOGA only
KBL SELECT
Function | KBL_ID
KBL | 1
NO KBL | 0
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
Int. K/B Matrix
SPI Flash ROM
SM Bus
GPIO
PECI
Share ROM
Compal Secret Data
2016/02/16
Deciphered Date
2017/02/16
Compal Electronics, Inc.
EC NPCE388
LA-D451P
Rev 1.0
Tuesday, February 16, 2016
Sheet 34 of 50

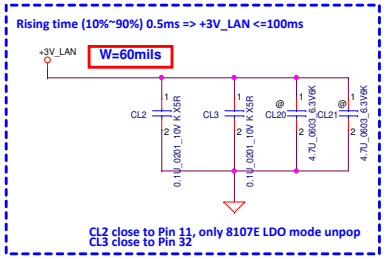


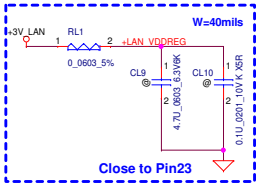



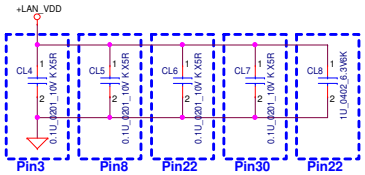

| | 1.0V Source | RL11 | CL15 |
|---|---|---|---|
| RTL8111H | LDO | O | O |
| RTL8107E | LDO | O | O |

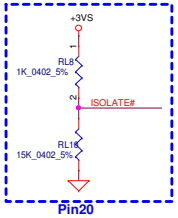
Please refer to the table above when using different 1.0V supply source.

LL1, CL16, and CL17 close to Pin24
( Should be place within 200 mils )

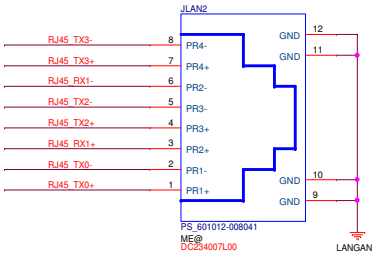


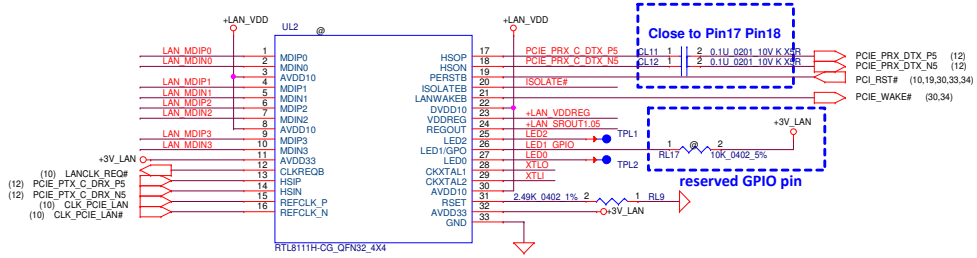




## RJ-45 CONN.

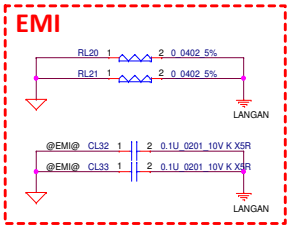


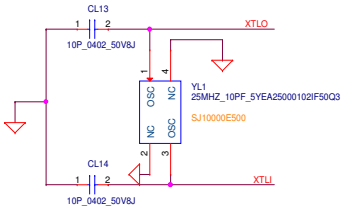




UL2
SA000086300
S IC RTL8107E-CG QFN 32P E-LAN CTRL
8107E@

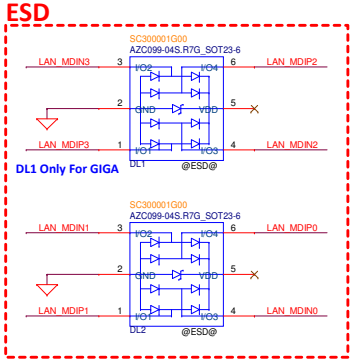
UL2
SA000080P00
S IC RTL8111H-CG QFN 32P E-LAN CTRL
8111H@

## EMI

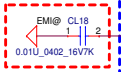


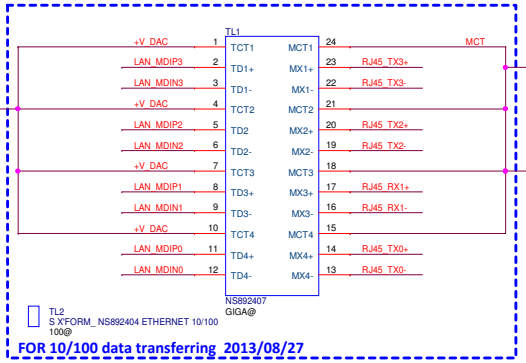




## ESD

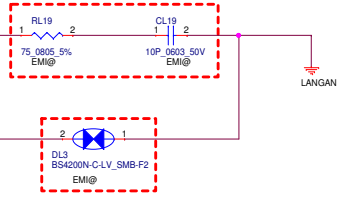



## EMI




## EMI




## EMI

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |

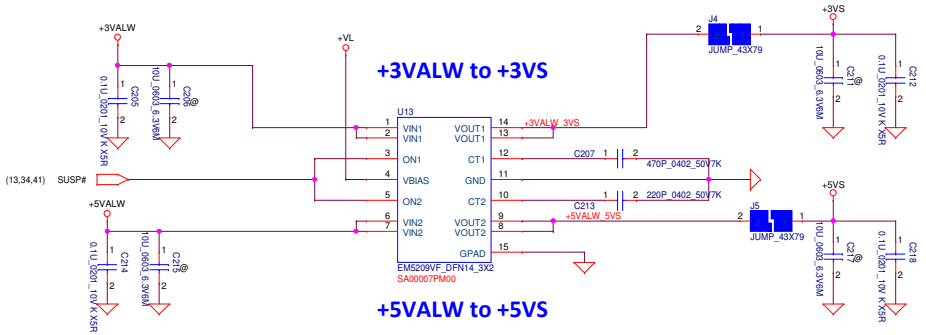


**Compal Electronics, Inc.**

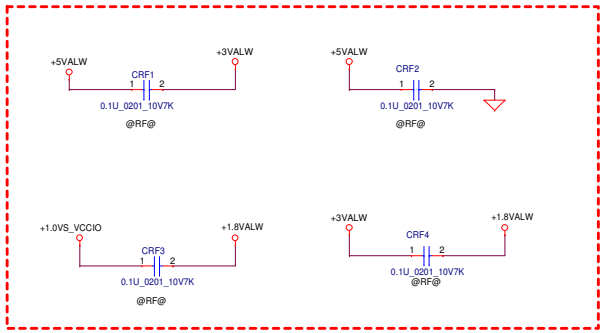
Title: LAN_RTL8111H / RTL8107E

| Size | Document Number | Rev |
|---|---|---|
| C | LA-D451P | 1.0 |

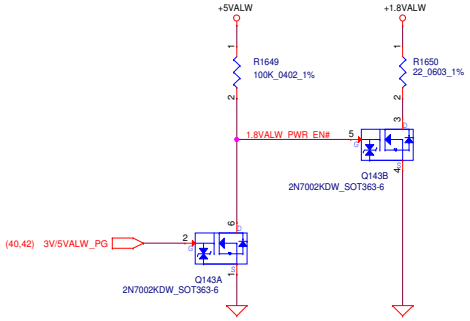
Date: Tuesday, February 16, 2016 | Sheet 35 of 50



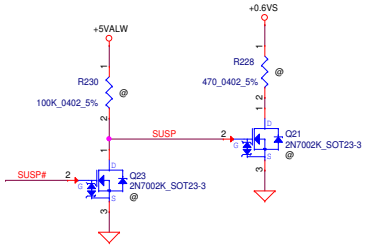

## RF




## For +1.8VALW Discharge




## For +0.6VS Discharge




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |



**Compal Electronics, Inc.**

Title: DC to DC

| Size | Document Number | Rev |
|---|---|---|
| C | LA-D451P | 1.0 |

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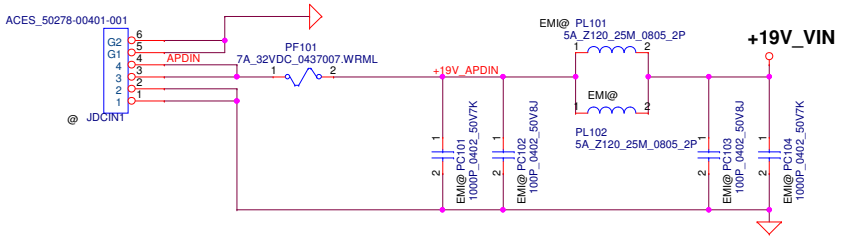
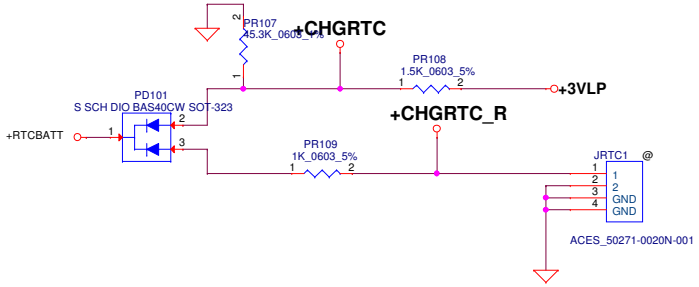



| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |

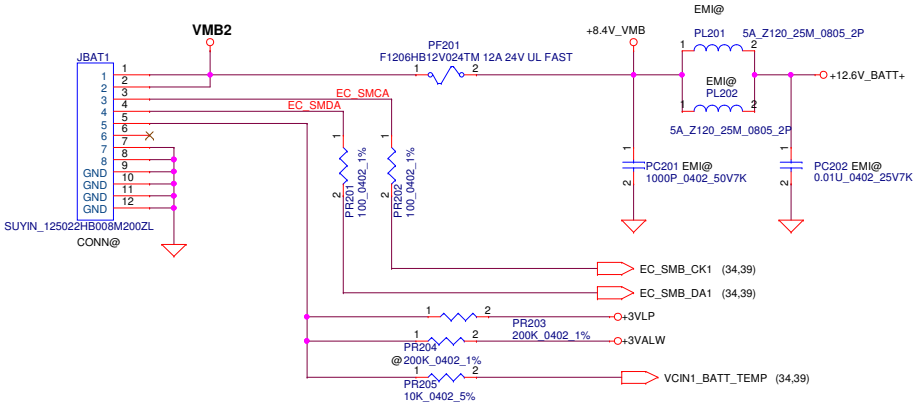


Compal Electronics, Inc.

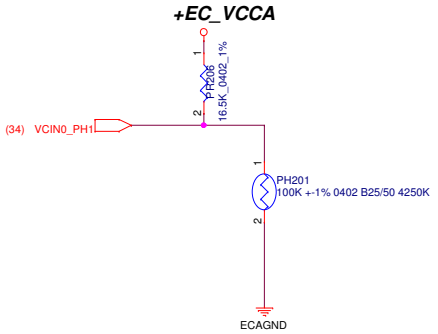
Title: PWR- DCIN / Vin Detector

| Size | Document Number | Rev |
|---|---|---|
| Custom | SKL | 1.0 |

Date: Tuesday, February 16, 2016 Sheet 37 of 50




***PH201 under CPU botten side :***
***CPU thermal protection at 93 +-3 degree C***
***Recovery at 56 +-3 degree C***




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |



Compal Electronics, Inc.

Title: PWR- BATTERY CONN/OTP

Size: Custom | Document Number: SKL | Rev: 1.0

Date: Tuesday, February 16, 2016 | Sheet 38 of 50

0x3CH <BIT9> PSYS current gain
Rs1 = 10mΩ and Rs2 = 5mΩ or Rs1 = 10mΩ and Rs2 = 10mΩ
BIT0 = 1.14uA/W
BIT1 = 0.285uA/W
==========
Rs1 = 20mΩ and Rs2 = 10mΩ or Rs1 = 20mΩ and Rs2 = 20mΩ
BIT0 = 2.28uA/W
BIT1 = 0.57uA/W

Ipsys = KPSYS x ( VADP x IADP + VBAT x IBAT )
R_Psys = 1.2V / Ipsys
KPSYS = 1.14uA/W
adapter wattage = 45W
Battery wattage = 40Wh
Ipsys = 1.14 x (45+40) = 96.9uA
R_Psys = 1.2V / 96.9uA = 12.3K-ohm.
==========
adapter wattage = 65W
Battery wattage = 40Wh
Ipsys = 1.14 x (65+40) = 119.7uA
R_Psys = 1.2V / 96.9uA = 10K-ohm.

**Design Notes**
For 45W/65W /90W system, 2S/3S/4S battery
Maximum Charging current 3.5A
Maximum Battery discharge power 55W
#Register Setting
1. 0X3DH bit10 set 0 (default 1) to enable turbo boost function
2. Disable turbo when AC only
#Circuit Design
1. ACLIM and CCLIM are devider voltage control.
2. Use 7X7 choke and 3X3 H/L side MOSFET
Charge current 3A
Power loss : 1.79W (H/S=0.227W,L/S=1.2738W,Choke=0.297W)
Power density : 0.61 (23X16)
#Protect function
1. ACOVP : VCC voltage > 24V
2. SMBus timeout : 0X3DH bit15 set 0 (default 0) to enable 175s(default).
3. ACOC : 0X3CH bit4 set1 release adapter limit function (default:Enable).
4. CHGOCP : based on charge current setting
5. BATOVP : 4.6V/Cell
6. BATLOWV : No.
7. TSHUT : 150C

Protection for reverse input

Vgs = 20V
Vds = 60V
Id = 250mA

PQ301 L2N7002WT1G_SC70-3
PR301 1M_0402_1%
PR302 3M_0402_5%

Rds(on) = 15.8mohm max
Vgs = 20V
Vds = 30V
ID = 10.5A (Ta=70C)

max Power loss 0.22W for 90W;0.12W for 65W system;0.05W for 45W
CSR rating: 1W
VCSIP-VCSIN spec < 81mV

Need check the SOA for inrush

PQ302 MDU1512RH_POWERDFN56-8-5
PQ303 AON7506_DFN33-8-5

+19V_VIN
+19V_P1
+19V_P2
B+

PR303 0.01_1206_1%
EMI@ PL301 1UH_2.8A_30%_4X4X2_F
+19VB_CHG

PC209 10U_0805_25V6K
PC204 10U_0805_25V6K
PC205 0.1U_0402_25V7K
EMI@ PC206 2200P_0402_25V7K

Co-lay jump and ISN choke.

CSIP_CHG_R
CSIN_CHG_R
@PR304 0_0402_5%
PR305 2_0402_5%
PC207 0.1U_0402_25V6

PR306 392K_0402_1%
ASGATE_CHG_R
PR307 4.02K_0402_1%
PR308 4.02K_0402_1%

PR729 and PR732 are ACDET setting base on your project to set.

PR309 100_0402_1%
+12.6V_BATT+

PQ304 AON7506_DFN33-8-5

Rds(on) = 32mohm max
Vgs = 20V
Vds = 30V
ID = 8A (Ta=70C)

@PC210 0.1U_0402_25V7K

PR310 49.9K_0402_1%
PC208 2200P_0402_50V7K

support Turbo boost : 2200P
no support Turbo boost : 0.1u

CMSRC_CHG
ASGATE_CHG
0.22U_0402_16V7K
PC209

PR311 100K_0402_1%
VDD_CHG
PR314 158K_0402_1%

(10,20,34) VCIN1_AC_IN

PU301 IC_ISL88739HRZ-T_QFN_32P_CHARGER

| | | | |
|---|---|---|---|
| 1 | ACIN | BOOT | 24 |
| 2 | ACOK | UGATE | 23 |
| 3 | SDA | PHASE | 22 |
| 4 | SCL | LGATE | 21 |
| 5 | PROCHOT# | VDDP | 20 |
| 6 | AMON | VDD | 19 |
| 7 | BMON | DCIN | 18 |
| 8 | PSYS | NTC | 17 |
| 33 | AGND | CSIP | 32 |
| 9 | PROG | CSIN | 31 |
| 10 | COMP | ASGATE | 30 |
| 11 | CCLIM | CMSRC | 29 |
| 12 | FSET | OPCN | 28 |
| 13 | BATGONE | OPCP | 27 |
| 14 | CSON | VBAT | 26 |
| 15 | CSOP | BGATE | 25 |
| 16 | ACLIM | | |

ACIN_CHG
(34,38) EC_SMB_DA1
(34,38) EC_SMB_CK1
(34) ADP_I
(34) DCHG_I
(45) PMON_SKYLAKE
(34) VCOUT1_PROCHOT#

PR313 0_0402_5%
PR320 0_0402_5%
@PR318 0_0402_5%
@PR321 0_0402_5%
AMON_ISL95520
BMON_ISL95520

PC218 1000P_0402_25V8J
PC219 1000P_0402_25V8J
Close to EC.

Follow adapter and battery wattage in Vsys current source.
Base on CPU Core VR design.
The resistor is pop on CPU VR schematic.

@ PR322 10K_0402_1%
PR326 0_0402_5% @

PR312 2.2_0603_5%
BST_CHG_R
PC211 0.22U_0603_25V7K
UG_CHG
LX_CHG
LG_CHG
VDDP_CHG
VDD_CHG

PQ305 AON7408L_DFN8-5
7X7X3
Isat: 6.5A
DCR: 28mohm
PL302 4.7UH_5.5A_20%_7X7X3_M
+12.6V_BATT_CHG

PQ306 AON7752_DFN3X3EP8-5

PR319 4.7_0402_5%
PC215 1U_0402_16V6K
PC216 1U_0402_16V6K
PR323 100K_0402_1%
PR324 10_1206_5%
PD102 LRB715FT1G_SOT323-3
VF = 0.38V
+19V_VIN
PC220 1U_0603_25V6

PR316 @0_0603_5%
PR339 @ 0_0603_5%
+12.6V_BATT+
BA

A31 connect to BA
Other team connect to batt conn

PR315 0.01_1206_1%
+12.6V_BATT+
PC212 10U_0805_25V6K
PC213 10U_0805_25V6K
PC214 10U_0805_25V6K

Support max charge 3.5A
Power loss: 0.245W
CSR rating: 1W
VCSPP-VCSON spec < 81mV

PQ307 LMUN5113T1G_SOT323-3
(10,34,41) PM_SLP_S4#
PQ308 LTC015EUBFS8TL_UMT3F
BA

For A31 only.
Turn off Charger IC on battery only.
Depend on customer design for system power consumption.

VDD=5V
VDD_CHG
PR328 200K_0402_1%
PR329 200K_0402_1%
CCLIM_CHG
ACLIM_CHG
PROG_CHG
COMP_CHG
FSET_CHG
PR325 10K_0402_1%

CSOP_CHG
PR331 2_0402_5%
CSOP_CHG_R
PC221 0.1U_0402_25V6
CSON_CHG
CSON_CHG_R
@PR336 0_0402_5%

Fs=729KHZ ~ +/- 15%

@ PR332 76.8K_0402_1%
@ PQ310 L2N7002WT1G_SC70-3
VCIN1_AC_2N
PR337 63.6K_0402_1%
U45W@
PR338 154K_0402_1%
PR335 182K_0402_1%
PR333 100_0402_1%
PR334 38.3K_0402_1%
@ PC222 560P_0402_50V7K
PC223 0.015U_0402_25V7K
PC224 10P_0402_25V8J

VCIN1_BATT_TEMP (34,38)
BATGONE(BATT_TEMP)
logic high: above 2.4V
logic low: under 0.8V

Hybrid boost power mode
Cell = 3s

(Rs1 = 10mΩ and Rs2 = 5mΩ or Rs1 = 20mΩ and Rs2 = 10mΩ).
CC_LIM = VccLIM / 64 x Rs2
==========
(Rs1 = 10mΩ and Rs2 = 10mΩ or Rs1 = 20mΩ and Rs2 = 20mΩ).
CC_LIM = VccLIM / 32 x Rs2
==========
AC_LIM = Vac_LIM / 32 x Rs1

PR337 U65W@ 76.8k_0402_1%

Adapter current limimed:
For U22(45W)_adp:
PR337=53.6k
For U23e(65W) and DIS_adp:
PR337=76.8k

Battery current limimed by CCLIm ~ 3.89A.
Adapter current limimed by ACLIm ~ 4.33A.
(PR779 and PQ741 are for change ACLIm when AC in)

Module model information
ISL95520_Hybrid_Boost_V2.mdd

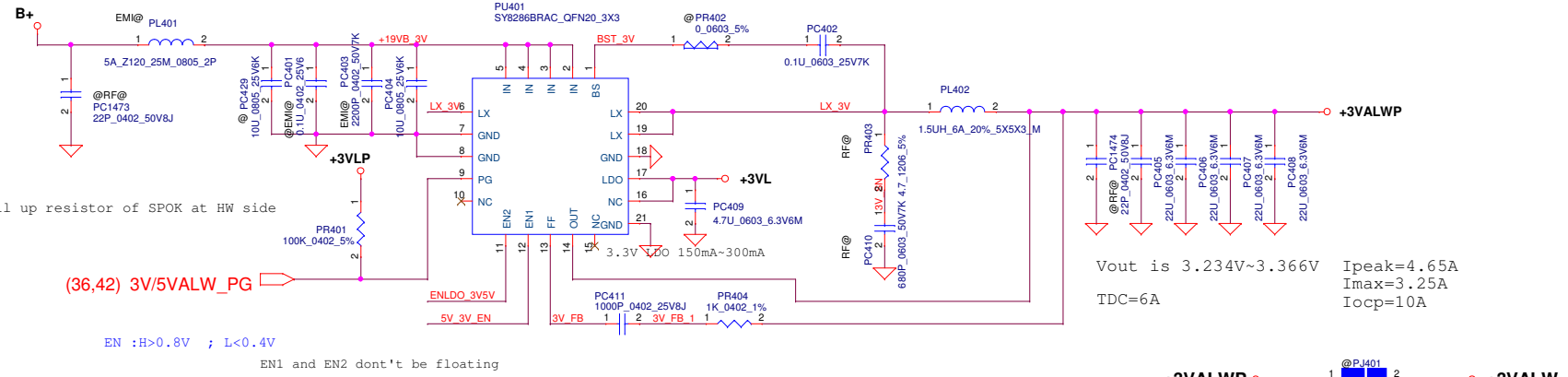
| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |



Compal Electronics, Inc.
Title: PWR_CHARGER
Size: | Document Number: | Rev: 1.0
Date: Tuesday, February 16, 2016 | Sheet 39 of 50

Module model information

SY8286B_V1.mdd



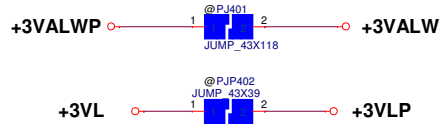

Check pull up resistor of SPOK at HW side

EN :H>0.8V ; L<0.4V

EN1 and EN2 dont't be floating

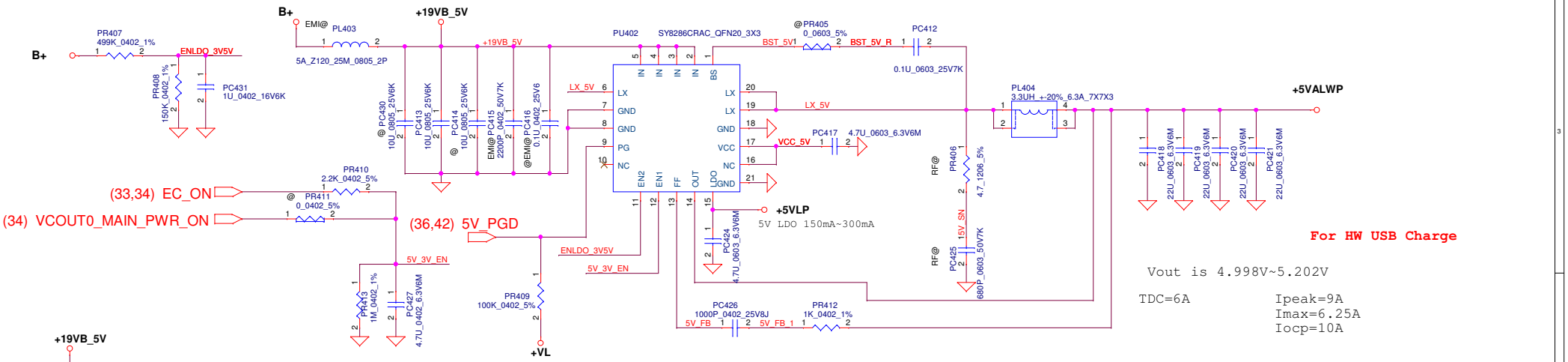
Vout is 3.234V~3.366V Ipeak=4.65A
Imax=3.25A
Iocp=10A

TDC=6A




Module model information

SY8286C_V1.mdd




For HW USB Charge

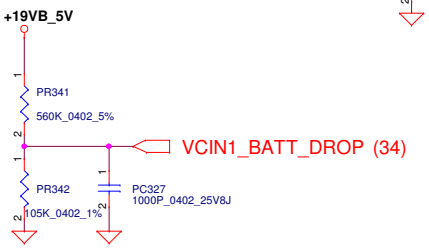
Vout is 4.998V~5.202V

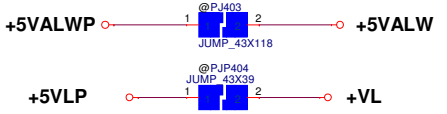
TDC=6A

Ipeak=9A
Imax=6.25A
Iocp=10A

EN :H>0.8V ; L<0.4V

EN1 and EN2 dont't be floating




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |

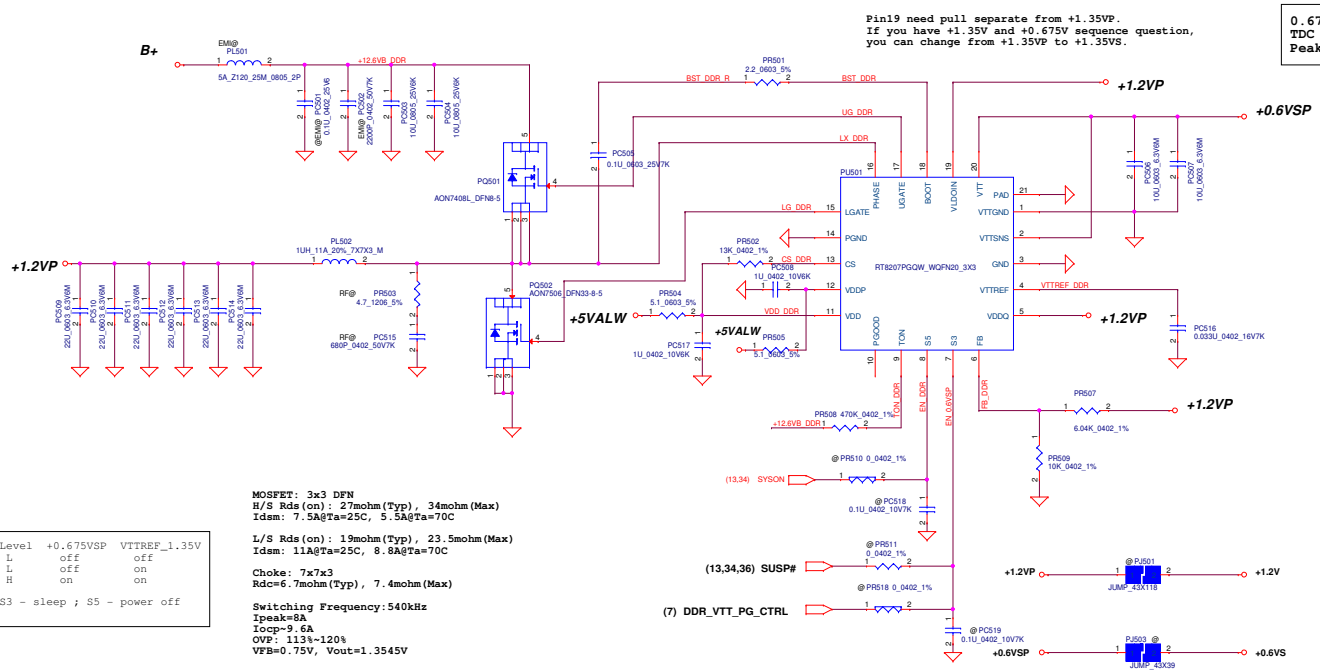


Compal Electronics, Inc.

Title: PWR- 3VALW/5VALW-SY8286B&C

Size: Custom | Document Number | Rev: 1.0

Date: Tuesday, February 16, 2016 | Sheet 40 of 50




Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question, you can change from +1.35VP to +1.35VS.

0.675Volt +/- 5%
TDC 0.7A
Peak Current 1A

| Mode | Level | +0.675VSP | VTTREF_1.35V |
|---|---|---|---|
| S5 | L | off | off |
| S3 | L | off | on |
| S0 | H | on | on |

Note: S3 - sleep ; S5 - power off

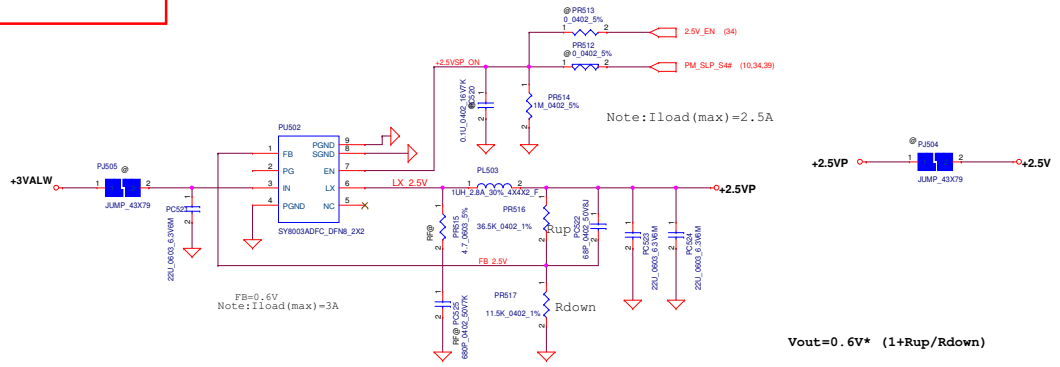
MOSFET: 3x3 DFN
H/S Rds(on): 27mohm(Typ), 34mohm(Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds(on): 19mohm(Typ), 23.5mohm(Max)
Idsm: 11A@Ta=25C, 8.8A@Ta=70C

Choke: 7x7x3
Rdc=6.7mohm(Typ), 7.4mohm(Max)

Switching Frequency:540kHz
Ipeak=8A
Iocp=9.6A
OVP: 113%~120%
VFB=0.75V, Vout=1.3545V

Module model information
SY8003A_V1.mdd




Vout=0.6V* (1+Rup/Rdown)

Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |



Compal Electronics, Inc.

Title: +1.2VP/+0.6VSP/+2.5VP

| Size | Document Number | Rev |
|---|---|---|
| Custom | LA-D451P | 1.0 |

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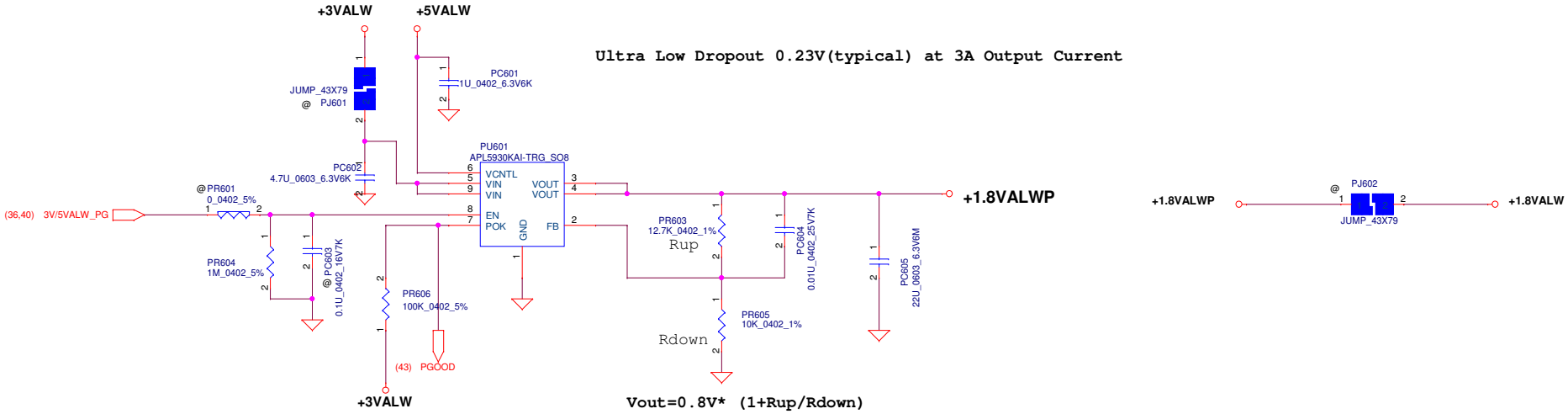
Module model information

APL5930_V2.mdd




| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |



Compal Electronics, Inc.

Title: +1.8V_PRIM

| Size | Document Number | Rev |
|---|---|---|
| Custom | | 1.0 |

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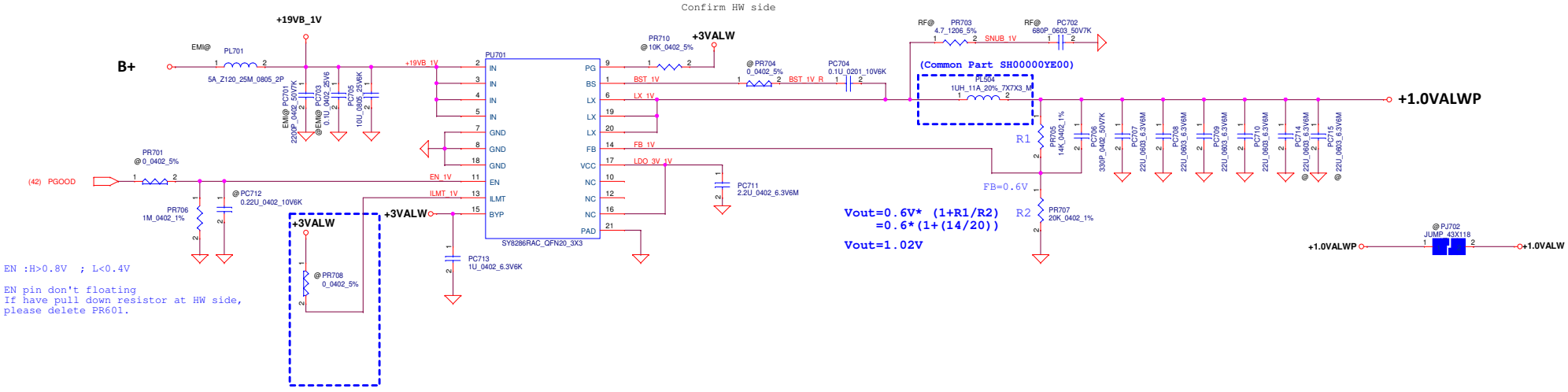
Module model information

SY8288_V1.mdd




EN :H>0.8V ; L<0.4V

EN pin don't floating
If have pull down resistor at HW side,
please delete PR601.

The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high.

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |



Compal Electronics, Inc.

Title: +1.0VS

| Size | Document Number | Rev |
|---|---|---|
| C | Z_SKL | 1.0 |

Date: Tuesday, February 16, 2016 Sheet 43 of 50

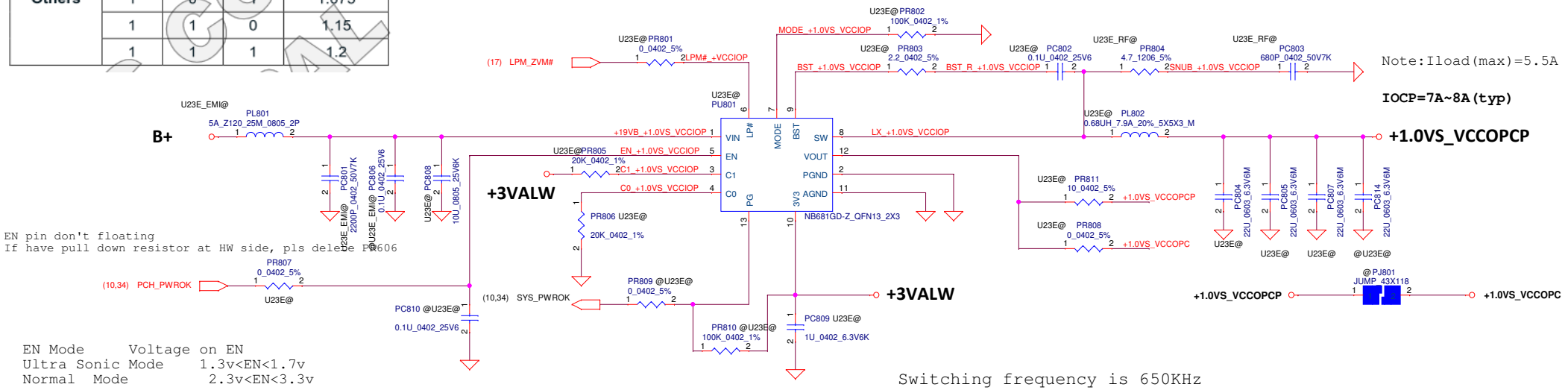
## Table 3—Control Bit Definitions

| | LP# | C1 | C0 | VOUT(V) |
|---|---|---|---|---|
| VCCIO | 0 | X | X | 0 |
| | 1 | 0 | 0 | 0.85 |
| | 1 | 0 | 1 | 0.875 |
| | 1 | 1 | 0 | 0.95 |
| | 1 | 1 | 1 | 0.975 |
| VCCPCH | 0 | X | X | 0.7 |
| | 1 | 0 | 0 | 0.8 |
| | 1 | 0 | 1 | 0.85 |
| | 1 | 1 | 0 | 0.9 |
| | 1 | 1 | 1 | 0.95 |
| EDRAM/ EOPIO | 0 | X | X | 0 |
| | 1 | 0 | 0 | 0.8(MSM) |
| | 1 | 0 | 1 | 0.95 |
| | 1 | 1 | 0 | 1 |
| | 1 | 1 | 1 | 1.05 |
| Others | 0 | X | X | 0 |
| | 1 | 0 | 0 | 1.0 |
| | 1 | 0 | 1 | 1.075 |
| | 1 | 1 | 0 | 1.15 |
| | 1 | 1 | 1 | 1.2 |



Module model information

NB681_V1.mdd






| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |

Title: +1.0VS_VCCOPC

Size: Custom | Document Number | Rev: 1.0

Date: Tuesday, February 16, 2016 | Sheet 44 of 50

# CPU CORE

**Due to U23e VCC_GT and GTX merged current spec is TBD in PDDG.**
**Please confirm FAE the setting of PRI23, PRI39 PRI63 for U23e GT and GTX merged.**

Module model information

NCP81208_U2223E_COLAY_V1A.mdd for IC portion

NCP81208_U2223E_COLAY_V1B.mdd for SW portion

Copy the schematic to new page,
the co-lay location maybe changed.

PRI2, PRI8 place near CPU side.
If the resisters are at HW side and POP. PRI2, PRI8 can be canceled.

PRI11, PRI16 place near CPU side.
If the resisters are at HW side and POP. PRI11, PRI16 can be canceled.

**RIOUT@GT:**
**U23e = 22.1K PRI23**
**U22 = 25.5K PRI23**

**RPH@GT:**
**U23e = 130K PRI929,PRI938**
**U22 =84.5K PRI929**

**For U22:**
**PRI943=De-pop**
**For U23e:**
**PRI943,PRI944=Pop**

**For U22:**
**PRI947=2K, PRI954=De-pop**
**For U23e:**
**PRI947=2K, PRI954=2K**

**For U22:**
**PCI923=De-pop**
**For U23e:**
**PCI923=0.1u**

U22 OCP@GT= 40A
RLIM@GT=12.4K ---->PRI39
U23e OCP@GT= 62A
RLIM@GT=12.4K ---->PRI39

RLIM= IoutLIMIT * Load line/10

U22 IccMAX@GT= 31A
RIccMAX2ph= 48.7K ---->PRI63
U23e IccMAX@GT= 56A
RIccMAX2ph= 87.6k ---->PRI63

RIccMAX2ph= (IccMAX2Ph+32)*200K Ohn/ 127

U22 Iout@GT= 31A
RIOUT@GT=25.5K ---->PRI23
U23e Iout@GT= 56A
RIOUT@GT=22.1K ---->PRI23

RIOUT= 2* RLIM /(10 *IOUTICCMAX * Load line)

U22 Load line@GT= 3.1m
RPH@GT=84.5K ---->PRI30,PRI38
U23e Load line@GT= 2m
RPH@VGT=130K ---->PRI30,PRI38

Load line= (RCS2+(RCS1*Rth/(RCS1+Rth)))
*IOUTTOTAL * DCR/RPH

472mV/120uA=3.933K
Active Point110 degreeC = 4.206K

NCP81208 Operating Frequency Rosc=24K
I/A and GT are 450KHz and SA is 450KHz

**RIccMAX2ph:**
**For U22:**
**PRI967=48.7K**
**For U23e:**
**PRI967=87.6K**

VBOOT:
22.1K for debuge setting.

**PSYS:**
Please confirm charger pull low resistance.
Charger side should be unpop.

IMVP8_EN
Upper Threshold > 0.8V
Lower Threshold < 0.3V

confirm with power sequence,
it need behind +5VS.

**PRI26 and PRI33 pull high resistor are pop at the end of VR SVID.**
**Other VR is unpop.**

IccMAX@SA= 5A
RIccMAX@SA= 15.8K --->PRI65

RIccMAX@SA= IccMAX*2V/10uA/64A

IOUTSP@SA= 5A
RIOUTSP@SA=69.8K --->PRI14

RIOUTSP= 2V/(gm*(Rth+RCSSP)*ICCMAX*DCR
/(RPHSP+Rth+RCSSP))

OCP@SA= 9.5A
RLIMSP@SA=24K --->PRI5

RLIMSP= 1.3V/(gm*(Rth+RCSSP)*IoutLIMIT*DCR
/(RPHSP+Rth+RCSSP))

Load line@SA= 10.3m
RDRPSP@SA=1.78K --->PRI4

RDRPSP= Load line*(RPHSP+Rth+RCSSP)
/(gm * DCR) /(Rth+RCSSP)

U22 Load line@VCORE= 2.35m
RDRPSP@VCORE=2.1K --->PRI56
U23e Load line@VCORE= 2.1m
RDRPSP@VCORE=1.87K --->PRI56

RDRPSP= Load line*(RPHSP+Rth+RCSSP)
/(gm * DCR) /(Rth+RCSSP)

IccMAX@VCORE= 28A
RIccMAX@VCORE= 87.6K --->PRI64

RIccMAX@VCORE= IccMAX*2V/10uA/64A

IOUTSP@VCORE= 28A
RIOUTSP@VCORE=64.9K --->PRI42

RIOUTSP= 2V/(gm*(Rth+RCSSP)*ICCMAX*DCR
/(RPHSP+Rth+RCSSP))

OCP@VCORE= 35A
RLIMSP@VCORE=33.4K --->PRI53

RLIMSP= 1.3V/(gm*(Rth+RCSSP)*IoutLIMIT*DCR
/(RPHSP+Rth+RCSSP))

PRI51, PRI58 place near CPU side.
If the resisters are at HW side and POP. PRI51, PRI58 can be canceled.

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |



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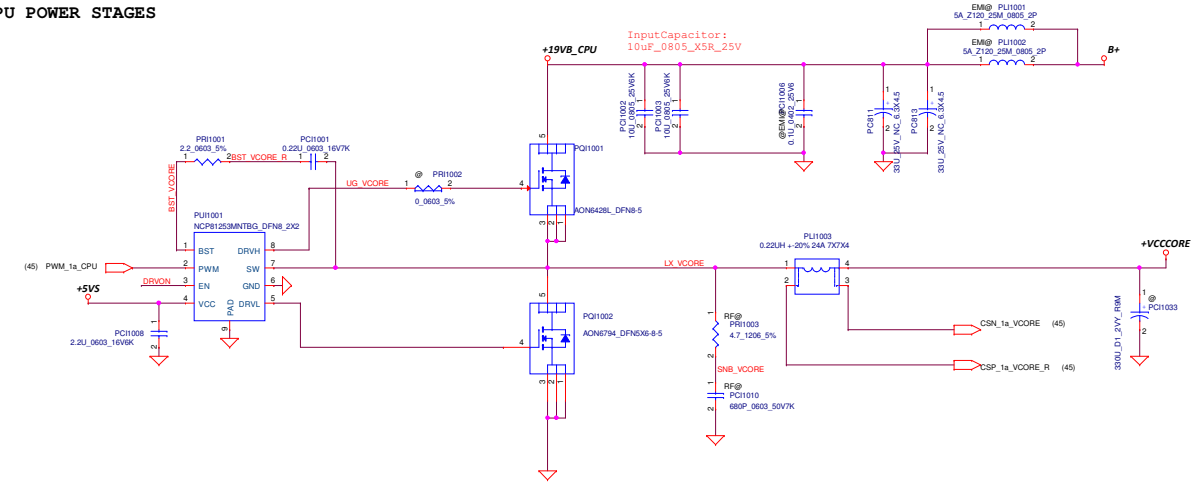
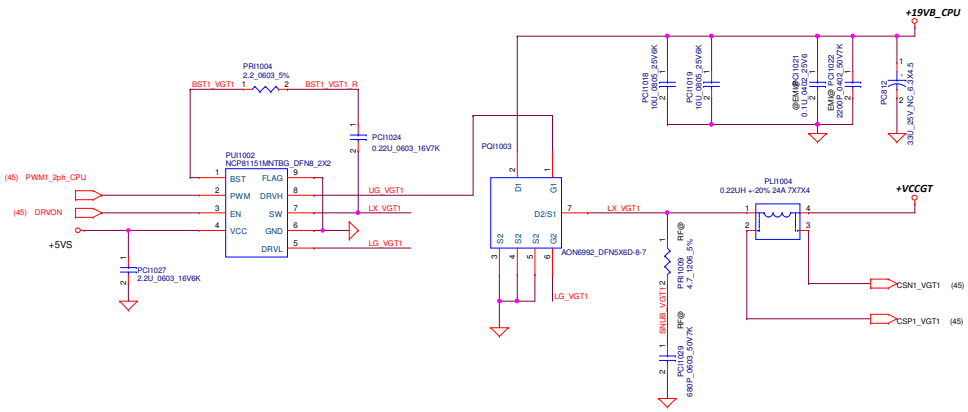
# CPU POWER STAGES



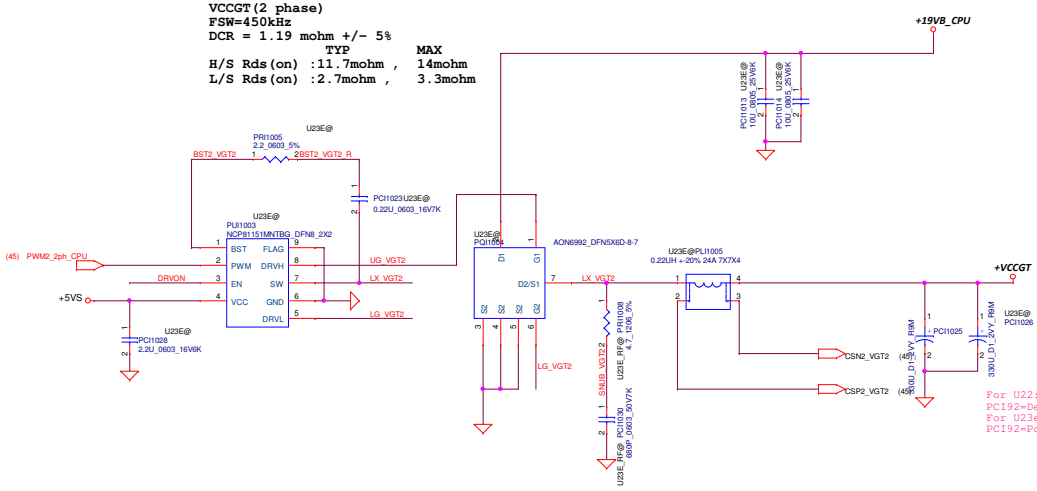

VCC_CORE
FSW=450kHz
DCR = 1.19 mohm +/- 5%

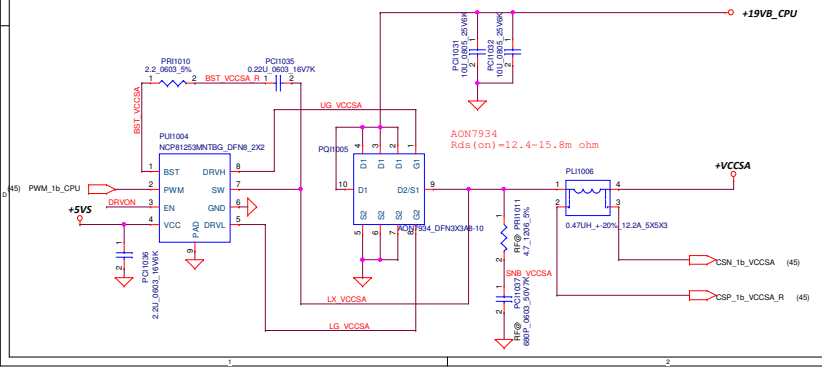
| | TYP | MAX |
|---|---|---|
| H/S Rds(on) | :11.7mohm , | 14mohm |
| L/S Rds(on) | :2.7mohm , | 3.3mohm |




VCCGT(2 phase)
FSW=450kHz
DCR = 1.19 mohm +/- 5%

| | TYP | MAX |
|---|---|---|
| H/S Rds(on) | :11.7mohm , | 14mohm |
| L/S Rds(on) | :2.7mohm , | 3.3mohm |




VCCSA
FSW=450kHz
DCR 6.2mohm(TYP), 6.51mohm(Max)

| | TYP | MAX |
|---|---|---|
| H/S Rds(on) | :12.4mohm , | 15.8mohm |
| L/S Rds(on) | :9.1mohm , | 11.6mohm |



| | | | |
|---|---|---|---|
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VCC_CORE Place on CPU Back Side @ V09
22U_0603 * 28 pcs +1U_0201*35 pcs

VCC_GT Place on CPU Back Side @ V09
22U_0603 * 29 pcs +1U_0201*12 pcs

+VCCCORE

+VCCGT

VCC_SA Place on CPU Back Side @ V09
22U_0603 * 9 (4 CPU back+8 outside)pcs + 1U_0201*7

PC1198 ,PC1199, PC1200是EMI的不上件元件

+VCCSA

+VCCGT

For PI simulation

| | | | |
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Module model information

ISL62771_CZ_GFX35W_V1A.mdd for IC portion
ISL62771_CZ_GFX35W_V1B.mdd for SW portion

VGA_M250=>Link +1.8VGS

VGA_M130=>Link +3VGS

VR_ON
High > 1.6V
Low < 1V

PH1002 near APU_CORE H/S mos
VRHOT Assert Threshold : 0.64V
TSENSE Bias Current : 30uA
PH1002=27.4K, 110C active
Reset Threshold: 0.66V, 98C active
110C Assert Threshold: PR1031=27.4K
100C Assert Threshold: PR1031=16.9K

PH1003 near GFX_CORE choke

PR1046 set 750 ohm to OCP 43.75A

PR1058=3.65K, PR1040=2.1K and
PR1046=604 to set loadline -2.1mV/A

PR1058=3.65K, PR1040=2.1K and
PR1046=604 to set loadline -2.1mV/A
while PR1046=594 to set OCP 57.16A
for EDC 45A application.

SH000010N00 (DCR:1.19mohm +/-5%)

+VGA_CORE

GFX_core
TDC 30(1H1L)
Peak Current 45A
OCP current > 45A
Load line -2.1mV/A
FSW=400kHz
DCR 1.19mohm +/-5%

| | TYP | MAX |
|---|---|---|
| H/S Rds(on) | :11.7mohm , | 14mohm |
| L/S Rds(on) | :2.7mohm , | 3.3mohm |

EN pin don't floating
If have pull down resistor at HW side, pls delete PR702

change PL601
SM01000C000 to comm
part SM01000P200

The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC15

Vout=0.6V* (1+Rup/Rdown)
=0.6*(1+(30.1/20))
Vout=1.503V

| | | | |
|---|---|---|---|
| Security Classification | Compal Secret Data | | |
| Issued Date | 2016/02/16 | Deciphered Date | 2017/02/16 |



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# Version change list (P.I.R. List)



| Item | Reason for change | PG# | Modify List | Date | Phase |
|---|---|---|---|---|---|
| 1 | 0ohm change to short pad | | PR316,PRI1002,PR318,PR321,PR336,PRI903,PRI906,PRI913,PRI917 | 2015.12.17 | SIT |
| 2 | ME 需求from 0603 change to 0402 | | PRI935,PRI912 | 2015.12.17 | SIT |
| 3 | | | | | |
| 4 | | | | 2015.09.14 | SDV |
| 6 | | P41 | | 2015.09.16 | SDV |
| 7 | | | | 2015.09.16 | SDV |
| 8 | | | | | |
| 9 | | | | 2015.10.08 | SIV |
| 10 | | | | 2015.10.22 | SIV |
| 11 | | | | 2015.10.22 | SIV |
| 12 | | | | | SIV |
| 13 | | | | | SIV |
| 14 | | | | 2015.10.22 | SIV |
| 15 | | | | | |
| 16 | | | | 2015.11.27 | SIT |
| 17 | | | | | |

# Version change list (P.I.R. List)



| Item | Reason for change | PG# | Modify List | Date | Phase |
|---|---|---|---|---|---|
| 1 | Camera couldn't be shutted down | P26 | adding C132,R119,Q4 for Camera power switch circuit | 2015/10/09 | SIV |
| 2 | Tuning charger sequence for avoid the conflict between +5VALW and +VL when booting on | P33 | adding C457,R338 for tuning Charger sequence in DC mode | 2015/10/09 | SIV |
| 3 | Audio shape fine tuning | P28 | changing cap size for shape fine-tuning | 2015/10/09 | SIV |
| 4 | Power reqeust | P15 | CC106 reserved for +1.0VS_VCCOPC | 2015/10/09 | SIV |
| 5 | RF reqeust | P24 | CV194 reserved for +1.5VGS | 2015/10/09 | SIV |
| 6 | ME request | P31 | changing H19 from 2P5 to 4P6 | 2015/10/09 | SIV |
| 7 | Intel design guide recommendation | P11 | chageing RC27,RC32 from 499 to 1k Ohms for TS screen pull-high | 2015/10/12 | SIV |
| 8 | 0 Ohm reduction | P13,21,22, 26,28,29,30, 31,35 | changing LV1,LV2,LV3,R121,R168,R311,RA2,RA42,RA43,RC136,RC137,RH142, RL11,RL18,RV5,RV6,RWL164 to R-short | 2015/10/13 | SIV |
| 9 | changing NOVO# pull-high from SB side to MB side | P34 | adding R1655 for NOVO# pull-high in MB side | 2015/10/13 | SIV |
| 10 | location renaming | P34 | location name changing from R2014 to R1656 | 2015/10/13 | SIV |
| 11 | keyboard matrix definition will change | P34 | reserving R1657 pull high to +3VS for EC_GPIO72 | 2015/10/13 | SIV |
| 12 | removing useless pull-high resistor | P18 | removing RD43 for DDR_DRAMRST# | 2015/10/13 | SIV |
| 13 | Common material use | P19,21 | changing QV16 to SB000013I00, UV2 to SA007080100 | 2015/10/13 | SIV |
| 14 | ME request | P26 | changing U5 to SA00008R900 | 2015/10/13 | SIV |
| 15 | Removing ACC_INT2_MB and ACC_INT2_SB routing reservation | P11,29 | adding T186,T187 for ACC_INT2, and ACC_INT2_MB, and deleting RC143,RC145 | 2015/10/13 | SIV |
| 16 | For Number LED feature | P34 | add BOM structure 15_NUM@ to R264 for 15" NUM LED | 2015/11/25 | SIT |
| 17 | new keyboard matrix definition implements | P34 | popping R1657 pull high to +3VS for EC_GPIO72 | 2015/11/25 | SIT |
| 18 | EC request to avoid YOGA's feature code mistake in S series | P34 | adding R1660 reserved for the pull high of TAB_SW# to fix display reverse issue in S series | 2015/12/09 | SIT |
| 19 | ESD request | P34 | adding C2143 for BATT_CHG_LED#,C2144 for BATT_LOW_LED# | 2015/12/11 | SIT |
| 20 | Power request for safety power test | P20 | reserving DV2 and RV374 for AC_BATT | 2015/12/11 | SIT |
| 21 | 0 Ohm reduction | P10,18,20, 26,28,34 | changing LA5~8,LV4,R132,R210,RC38,RD138,RD139,RD200,RD45,RV194 to R-short | 2015/12/11 | SIT |
| 22 | KBL circuit cost-down | P32,34 | adding RKBL4 to un-pop QKBL122 for cost-down, RKBL3 from 100k to 0 , modifying @ to RKBL2,R324and CKBL907, KBL@ to RKBL1, reserving R1665 for +3VS pull-high of KB_BL_PWM | 2015/12/11 | SIT |
| 23 | USB Charger tuning for sequence and control pins | P33 | changing @ to C457,R338,R1647,adding R1658,R1659 | 2015/12/11 | SIT |
| 24 | SUSP# leakage problem | P34 | adding a pull-down resistor R1664 for SUSP# | 2015/12/11 | SIT |
| 25 | DFX reqeust | P26,33 | removing common-mode choke locations L6,L13,L15,L17,L18 | 2015/12/11 | SIT |
| 26 | SUSP# leakage problem | P34 | adding a pull-down resistor R1664 for SUSP# | 2015/12/11 | SIT |
| 27 | Removing ISH reservation | P11,29,34 | removing R1653,R1654,RC140,RC141,T186,T187, and changing net ACC_INT1 to MB_ID | 2015/12/11 | SIT |
| 28 | Crystal cap fine tuning | P20 | changing CV19,CV20 to 8.2p | 2015/12/11 | SIT |
| 29 | Changing CPU's part numbers | P06 | changing CPU part number : SA00009E500 to SA00009E520, SA00009E630 to SA00009E610 | 2015/12/21 | SIT |
| 30 | For ME request to fix HDD shock issue | P31 | changing H7 from 4p6 to 6p0 | 2016/02/15 | SVT |



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