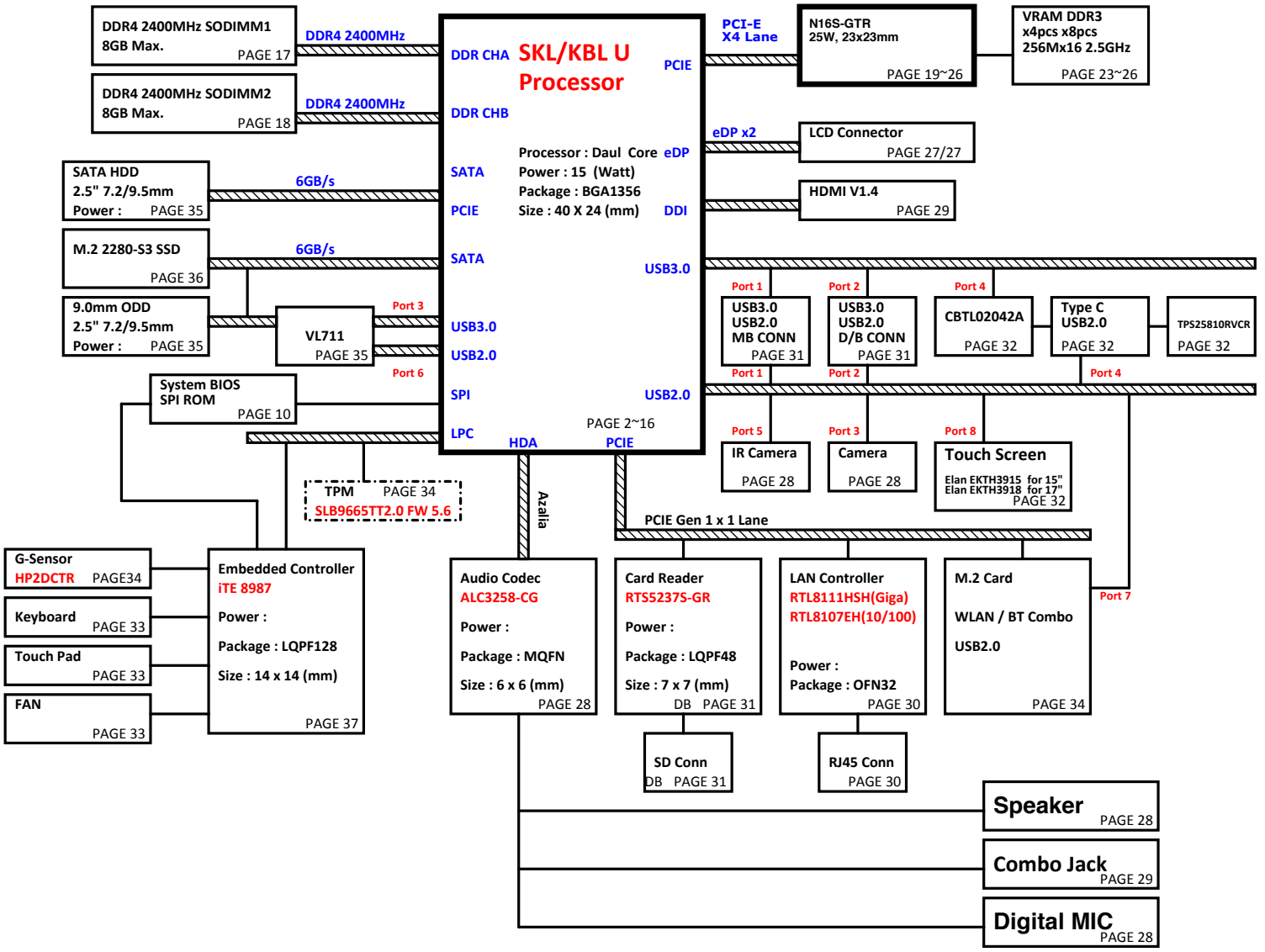
NFL 2SPD DIS/UMA (15/17")
Intel SKL/KBL ULT Platform Block Diagram

PCB 8L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : IN3(High)
LAYER 7 : SGND1
LAYER 8 : BOT



PROJECT : G74A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

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NB5

+3V 4,10,11,12,13,14,15,17,18,19,20,21,27,28,29,30,31,32,33,34,35,36,37,43,46,51
+1.0V 4,6,37,42
+VCCSTPLL 4,5,6,9,42,43

HDMI

U1A — SKL_ULT — DDI — EDP — DISPLAY SIDEBANDS — 1 OF 20 — *SKL_ULT — REV = 1

29	IN_D2#	IN_D2#	E55 DDI1_TXN[0]
29	IN_D2	IN_D2	F55 DDI1_TXP[0]
29	IN_D1#	IN_D1#	E58 DDI1_TXN[1]
29	IN_D1	IN_D1	F58 DDI1_TXP[1]
29	IN_D0#	IN_D0#	F53 DDI1_TXN[2]
29	IN_D0	IN_D0	G53 DDI1_TXP[2]
29	IN_CLK#	IN_CLK#	F56 DDI1_TXN[3]
29	IN_CLK	IN_CLK	G56 DDI1_TXP[3]

C50 DDI2_TXN[0], D50 DDI2_TXP[0], C52 DDI2_TXN[1], D52 DDI2_TXP[1], A53 DDI2_TXN[2], B53 DDI2_TXP[2], D51 DDI2_TXN[3], C51 DDI2_TXP[3]

29	SDVO_CLK	L13 GPP_E18/DDPB_CTRLCLK
29	SDVO_DATA	L12 GPP_E19/DDPB_CTRLDATA
TP2	DDPC_CTRLDATA	N7 GPP_E20/DDPC_CTRLCLK
		N8 GPP_E21/DDPC_CTRLDATA
TP3	DDPD_CTRLDATA	N11 GPP_E22/DDPD_CTRLCLK
		N12 GPP_E23/DDPD_CTRLDATA
+VCCIO	EDP_RCOMP R3 24.9_1%_4	E52 EDP_RCOMP

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Justsurport FHD 1920x1080

C47	EDP_TXN[0]	INT_EDP_TXN0	INT_EDP_TXN0 27
C46	EDP_TXP[0]	INT_EDP_TXP0	INT_EDP_TXP0 27
D46	EDP_TXN[1]	INT_EDP_TXN1	INT_EDP_TXN1 27
C45	EDP_TXP[1]	INT_EDP_TXP1	INT_EDP_TXP1 27
A45	EDP_TXN[2]		
B45	EDP_TXP[2]		
A47	EDP_TXN[3]		
B47	EDP_TXP[3]		
E45	EDP_AUXN	INT_EDP_AUXN	INT_EDP_AUXN 27
F45	EDP_AUXP	INT_EDP_AUXP	INT_EDP_AUXP 27
B52	EDP_DISP_UTIL	EDP_DISP_UTIL1 — TP1*	
G50	DDI1_AUXN		
C50	DDI1_AUXP		
E48	DDI2_AUXN		
F48	DDI2_AUXP		
G46	DDI3_AUXN		
F46	DDI3_AUXP		
L9	GPP_E13/DDPB_HPD0	HDMI_HPD_CON	HDMI_HPD_CON 29
L7	GPP_E14/DDPC_HPD1		
L6	GPP_E15/DDPD_HPD2		
N9	GPP_E16/DDPE_HPD3		
C10	GPP_E17/EDP_HPD	ULT_EDP_HPD	ULT_EDP_HPD 27
R12	EDP_BKLTEN	PCH_LVDS_BLON	PCH_LVDS_BLON 27
R11	EDP_BKLTCTL	PCH_DPST_PWM	PCH_DPST_PWM 27
U13	EDP_VDDEN	PCH_DISP_ON	PCH_DISP_ON 27

Reserve EDP_HPD opposites circuit!

+3V — R1 *10K/F_4 — ULT_EDP_HPD — R2 100K_4

37,43 H_PROCHOT# — R4 499/F_4 — 37 EC_PECI — 37 PM_THRMTRIP#

U1D — SKL_ULT — CPU MISC — JTAG — 4 OF 20 — *SKL_ULT — REV = 1

Need apply PN

CATERR#	D63	CATERR#
EC_PECI	A54	PECI
PROCHOT#	C65	PROCHOT#
PM_THRMTRIP#	C63	THERMTRIP#
	A65	SKTOCC#
TP127 XDP_BPM0	C55	BPM#[0]
TP128 XDP_BPM1	D55	BPM#[1]
	B55	BPM#[2]
	C56	BPM#[3]
TP113 3D_FW_GPIO_R	A6	GPP_E3/CPU_GP0
TP4 CPU_GP1	A7	GPP_E7/CPU_GP1
TP5 CPU_GP2	BA5	GPP_B3/CPU_GP2
TP6 CPU_GP3	AY5	GPP_B4/CPU_GP3
R8 49.9/F_4 PROC_POPIRCOMP	AT16	PROC_POPIRCOMP
R11 49.9/F_4 PCH_OPI_RCOMP	AU16	PCH_OPIRCOMP
R12 49.9/F_4 EDRAM_OPIO_RCOMP	H66	OPCE_RCOMP
R14 49.9/F_4 EOPIO_RCOMP	H65	OPC_RCOMP

	PROC_TCK	B61	XDP_TCK0
	PROC_TDI	D60	XDP_TDI_CPU — TP999
	PROC_TDO	A61	XDP_TDO_CPU
	PROC_TMS	C60	XDP_TMS_CPU — TP998
	PROC_TRST#	B59	PROC_TRST#
	PCH_JTAG_TCK	B56	JTAG_TCK_PCH
	PCH_JTAG_TDI	D59	JTAG_TDI_PCH
	PCH_JTAG_TDO	A56	JTAG_TDO_PCH
	PCH_JTAG_TMS	C59	JTAG_TMS_PCH
	PCH_TRST#	C61	XDP_TRST#_CPU
	JTAGX	A59	JTAGX_PCH

XDP_TRST#_CPU — R863 *0_4/S — PROC_TRST#

+VCCSTPLL — R6 *49.9/F_4 — CATERR#

+1.0V — R9 *0_4/S

R10	*51_4	JTAGX_PCH
R13	51_4	JTAG_TMS_PCH
R15	51_4	JTAG_TDI_PCH
R16	51_4	JTAG_TDO_PCH
R18	51_4	JTAG_TCK_PCH

Close to Chipset

Close to EC

+VCCSTPLL — PM_THRMTRIP# — R5 1K_4

Processor pull-up (CPU)
TO BE REPLACED WITH 1K OHMS FOR SKL .
470 OHM IS FOR I/P

PLACE NEAR CPU

+1.0V

XDP_TMS_CPU	R17	*51_4
XDP_TDI_CPU	R19	*51_4
XDP_TDO_CPU	R20	*51_4

+1.0V

H_PROCHOT#	R21	1K_4
XDP_TCK0	R22	51_4
XDP_TRST#_CPU	R23	51_4

NB5

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	02 -- SKYPAKE 1/15 (eDP/DDI)	1A

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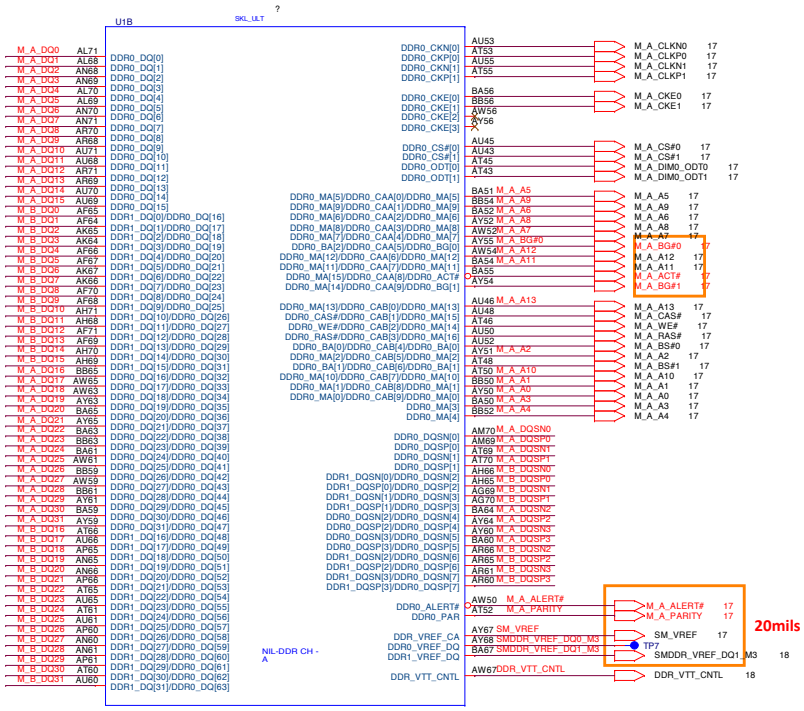
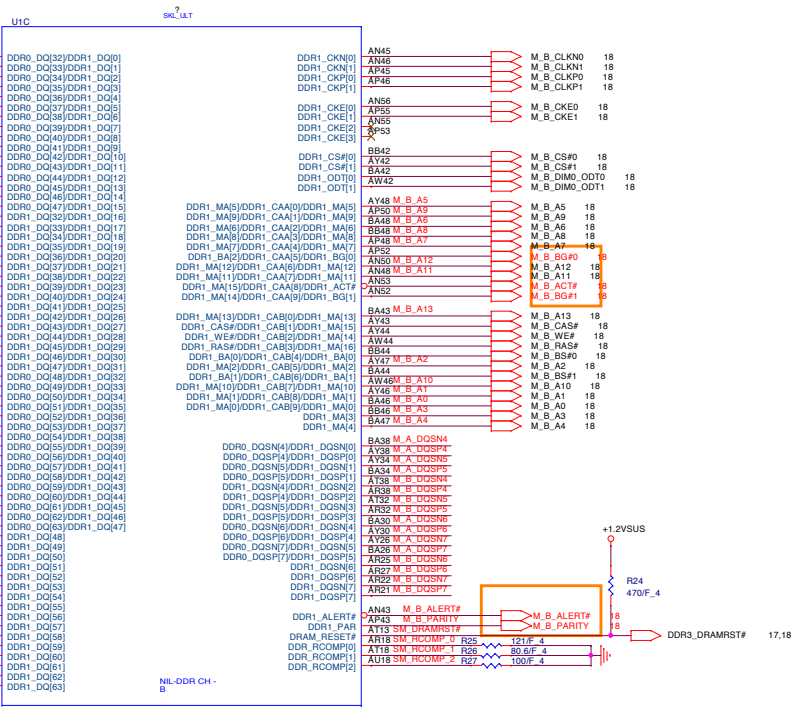
SkyLake ULT Processor (DDR4)

17 M_A_DQSN[7:0]
17 M_A_DQSP[7:0]
18 M_B_DQSN[7:0]
18 M_B_DQSP[7:0]
17 M_A_DQ[63:0]
18 M_B_DQ[63:0]

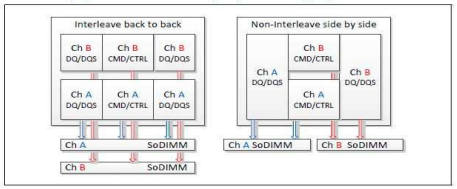
+1.2VSUS 6,17,18,40,42,48





20mils width

Interleave (IL) and Non-Interleave (NIL) Modes Mapping



PROJECT : G74A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	03 – SKYLAKE 2/15(DDR4 I/F)	1A

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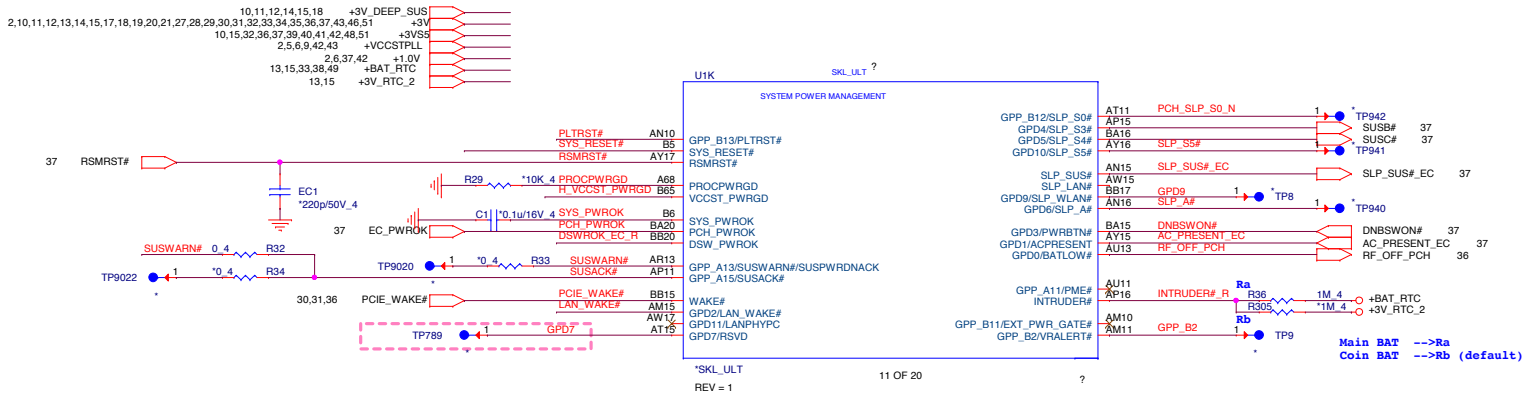
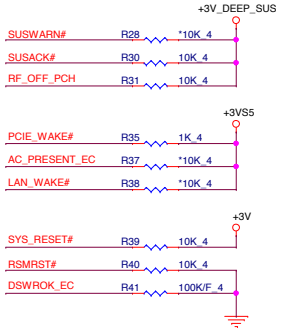
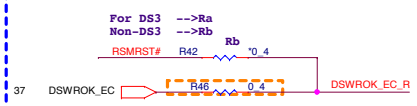


PCH Pull-high/low(CLG)

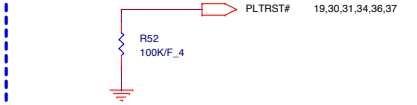


For DS3 Sequence

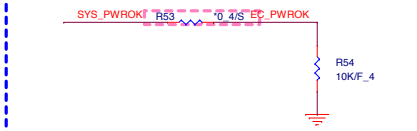


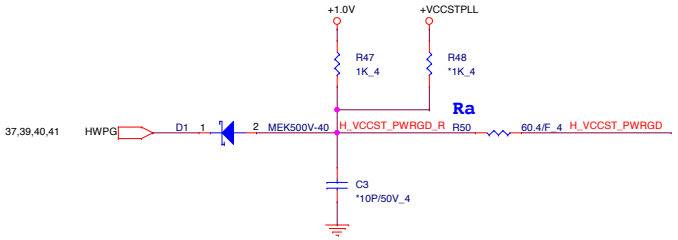
PLTRST#(CLG)

Check Rise/Fall time less than 100ns

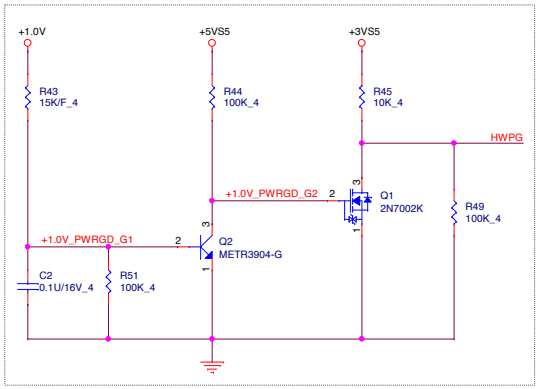


System PWR_OK(CLG)





Ra close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"



NB5	PROJECT : G74A Quanta Computer Inc.	
Size: Custom	Document Number: 04 -- SKYLAKE 3/15(PowerManger)	Rev: 1A
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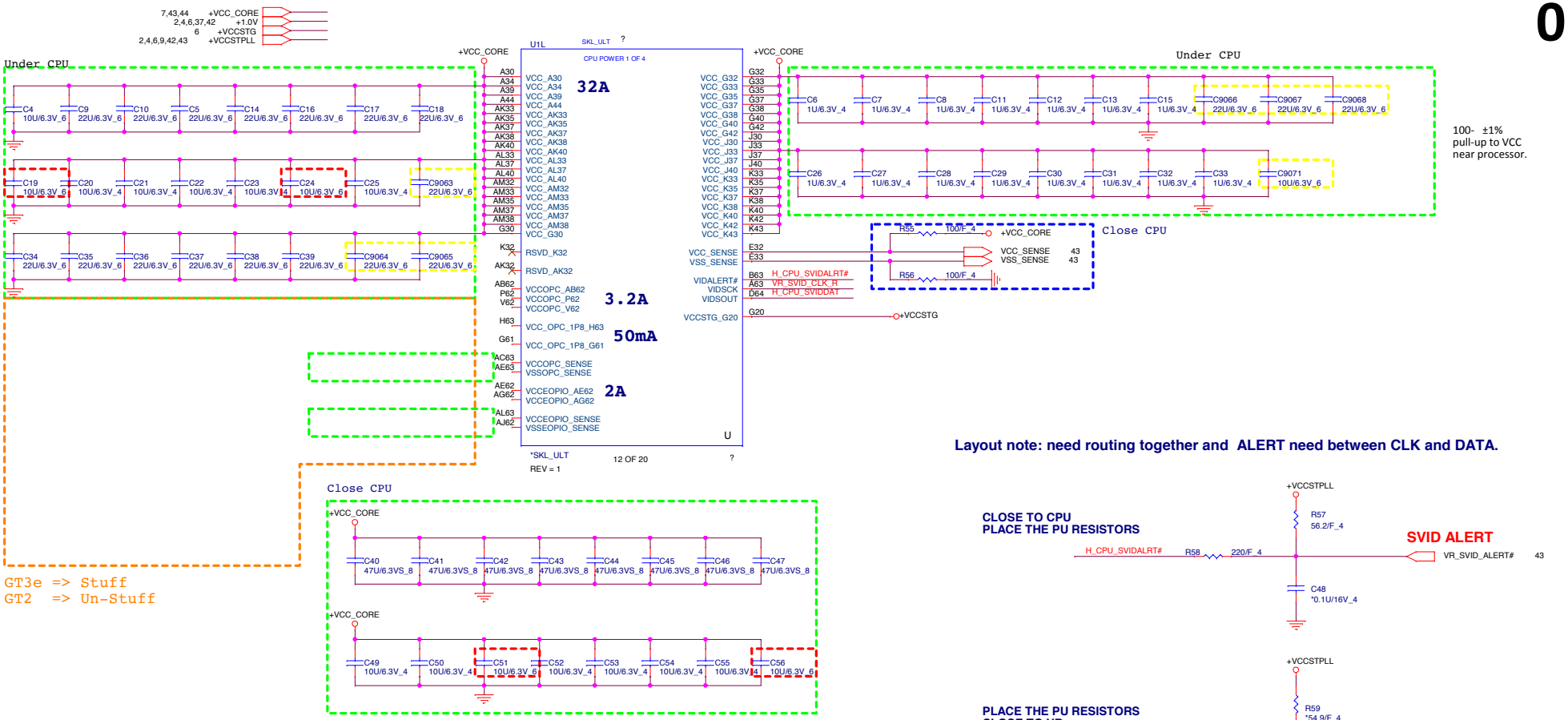
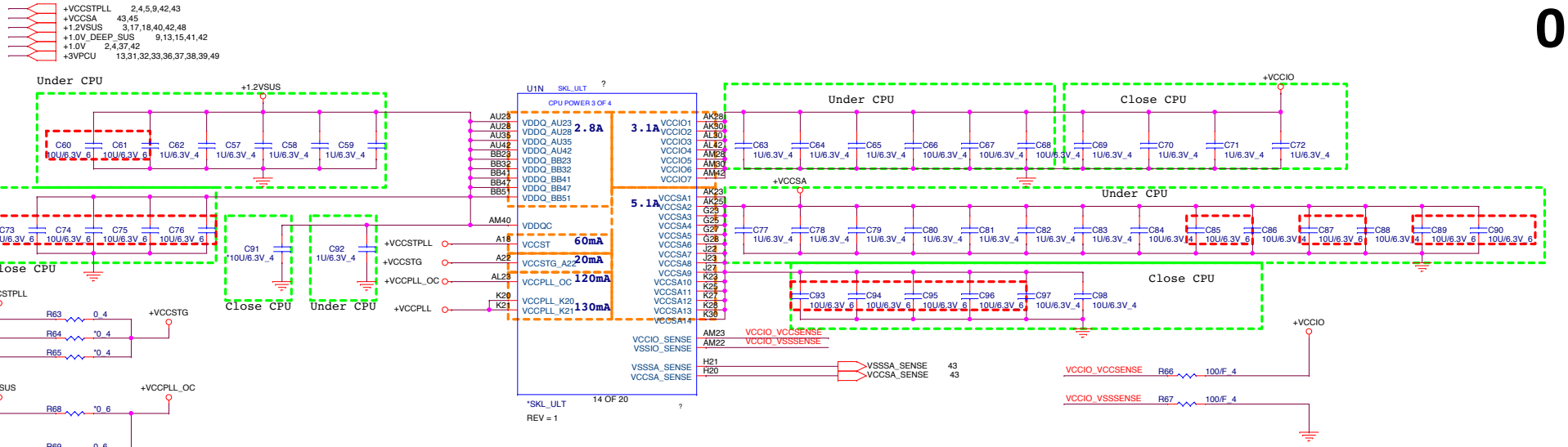


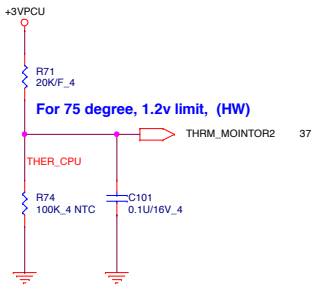
Layout note: need routing together and ALERT need between CLK and DATA.

Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
$V_{CC_{GT}}$	Processor Graphics Power Rails	SVID
$V_{CC_{GTX}}$	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
$V_{CC_{SA}}$	System Agent Power Rail	SVID/Fixed (SKU dependent)
$V_{CC_{IO}}$	IO Power Rail	Fixed
$V_{CC_{ST}}$	Sustain Power Rail	Fixed
$V_{CC_{PLL}}$	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
$V_{CC_{OPC}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{OPC\_1P8}}$	Processor OPC power rail (available only in SKU's with OPC)	Fixed
$V_{CC_{EOPIO}}$	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

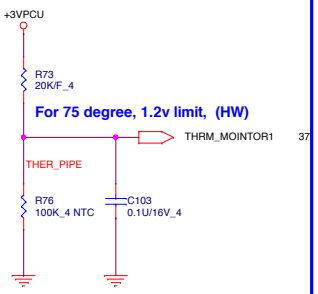


IO Thrm Protect

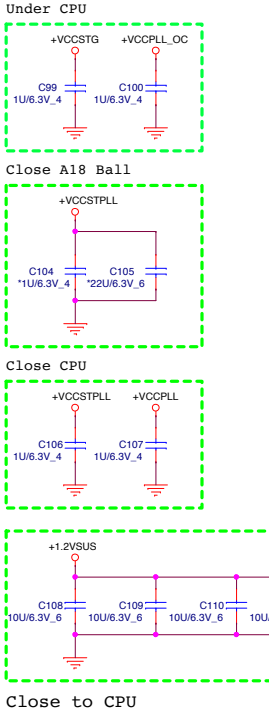
For PIPE USE

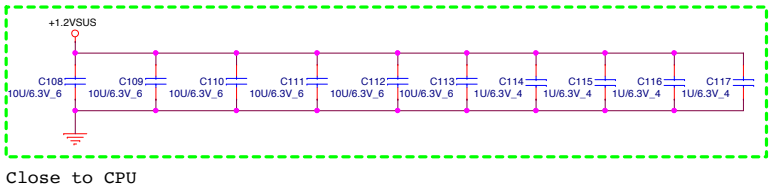


For CPU USE



Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed





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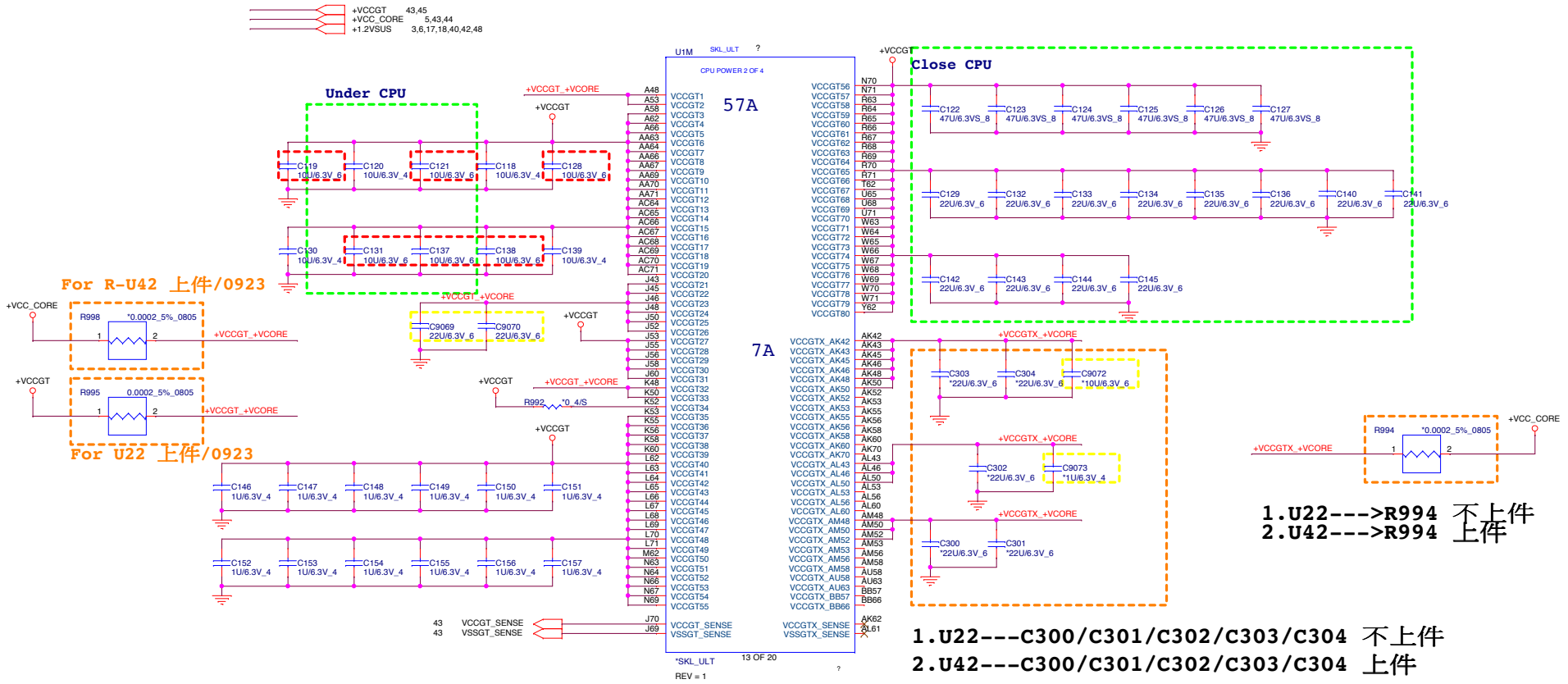
Quanta Computer Inc.	
Size: Custom	Document Number: 06 -- SKYLAKE 5/15 (POWER-2)
Rev: 1A	
Date: Wednesday, January 11, 2017	Sheet 6 of 51



1.U22--->R994 不上件
2.U42--->R994 上件

1.U22---C300/C301/C302/C303/C304 不上件
2.U42---C300/C301/C302/C303/C304 上件

Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

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Quanta Computer Inc.
Size: Custom | Document Number: 07 -- SKYLAKE 6/15 (POWER-3) | Rev: 1A
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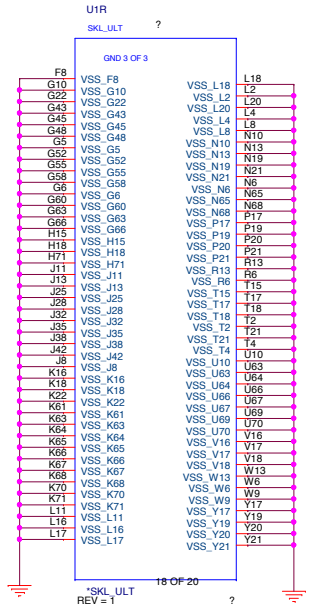

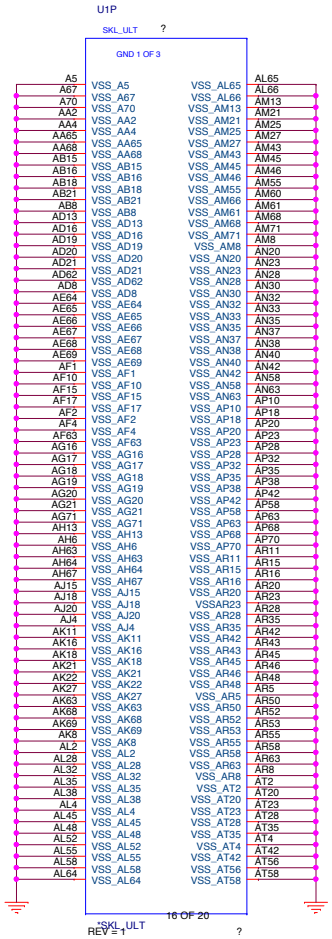

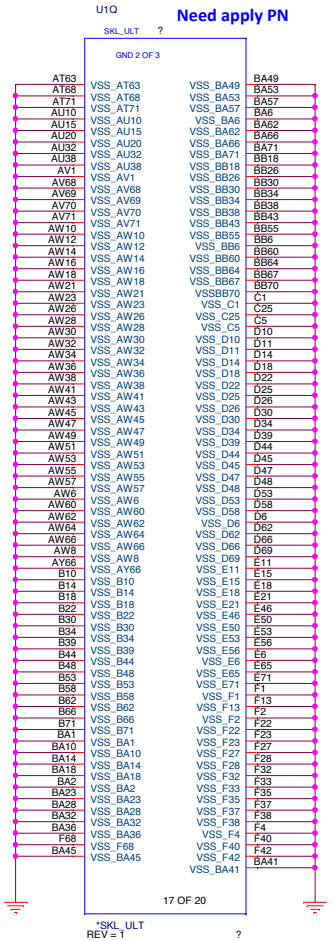

NB5

PROJECT : G74A

Quanta Computer Inc.

Size	Document Number	Rev
Custom	08 -- SKYLAKE 7/15 (GND)	1A

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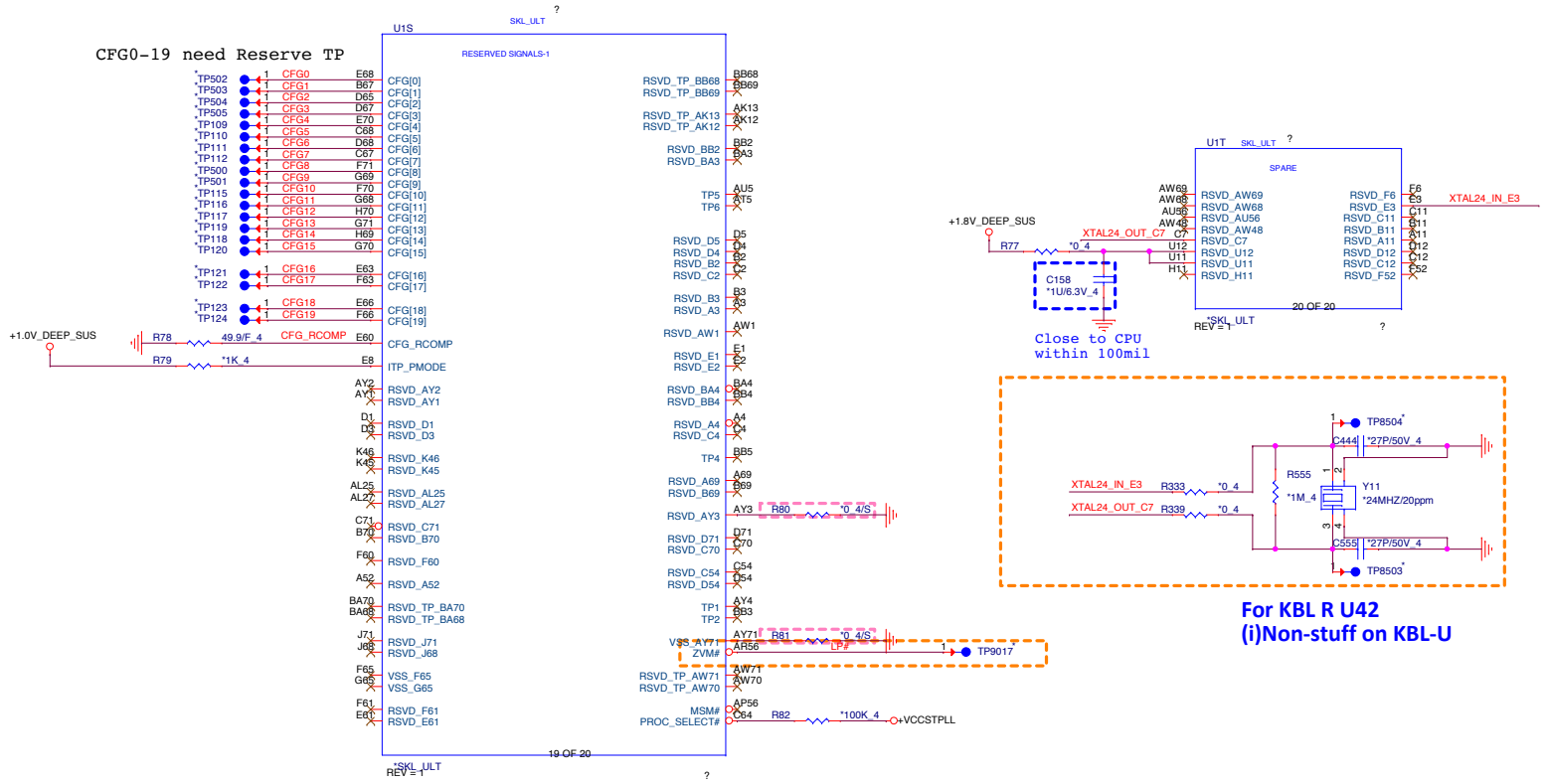

Processor Strapping The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physcial Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R83 *1K_4
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R84 1K_4

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	09 -- SKYLAKE 8/15 (RSV)	1A

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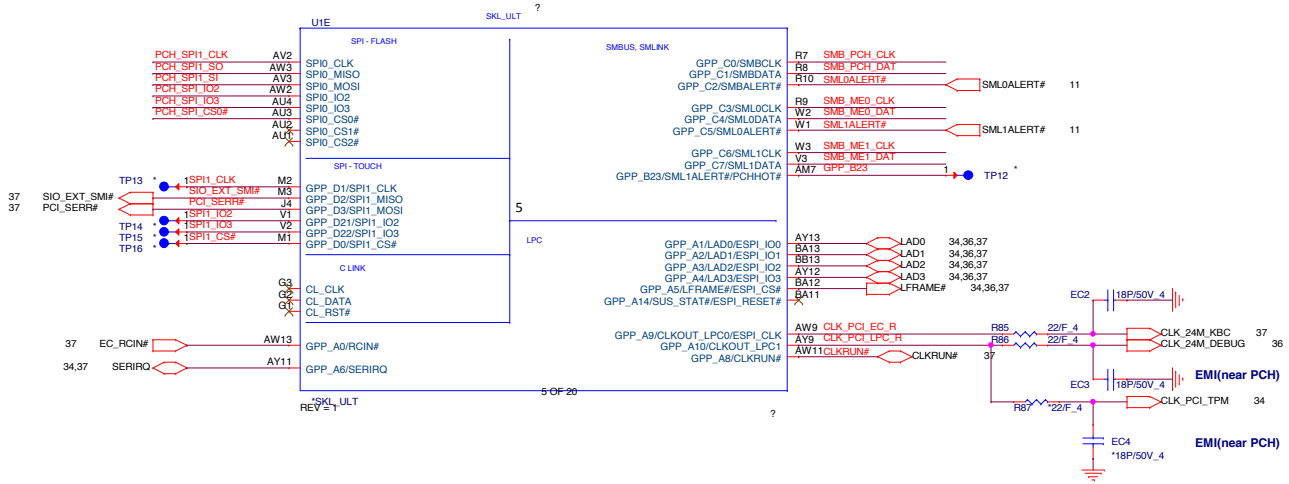
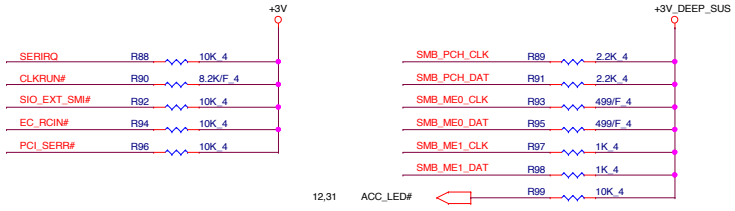
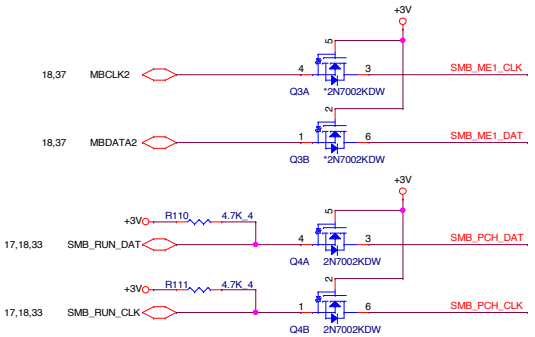
+3V_DEEP_SUS 4,11,12,14,15,18
+3V 2,4,11,12,13,14,15,17,18,19,20,21,27,28,29,30,31,32,33,34,35,36,37,43,46,51
+5V 27,28,29,33,35,51
+1.0V 2,4,6,37,42
+3VS5 4,15,32,36,37,39,40,41,42,48,51



GPIO Pull UP



SMBus/Pull-up(CLG)



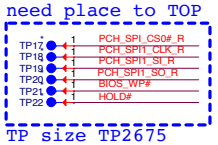
CPU heat pipe local thermal sensor
DDR thermal sensor
EC

Touch Pad
XDP
DDR4

PCH SPI ROM(CLG)

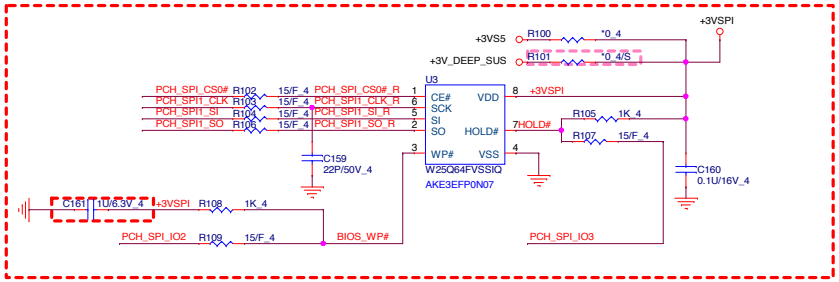
Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

need place to TOP



TP size TP2675

PCH SPI ROM(CLG)



P/N DFHS08FS023 (Socket)

NB5	PROJECT : G74A Quanta Computer Inc.	
Size: Custom	Document Number: 10 -- SKYLAKE 09/15(SPI/LPC/SM)	Rev: 1A
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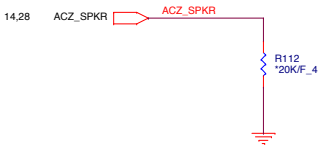
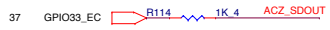
Functional Strap Definitions

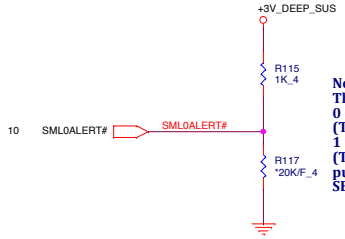
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET



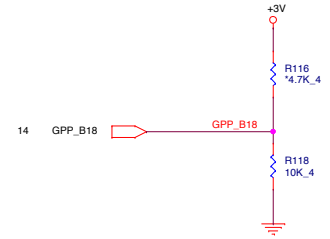
TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD

No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY. This function is useful when running ITP/XDP.

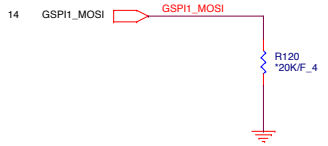




No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.

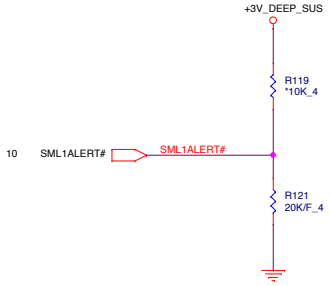


No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode
(PCH will disable the TCO Timer system reboot feature).
This function is useful when running ITP/XDP.



No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.

Bit 10	Boot BIOS Destination
0	SPI
1	LPC



No Boot:
The signal has a weak internal pull-down.
0 = LPC Is selected for EC.
1 = eSPI Is selected for EC.

NB5

PROJECT : G74A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	11 -- SKYLAKE 10/15(HDA)	1A

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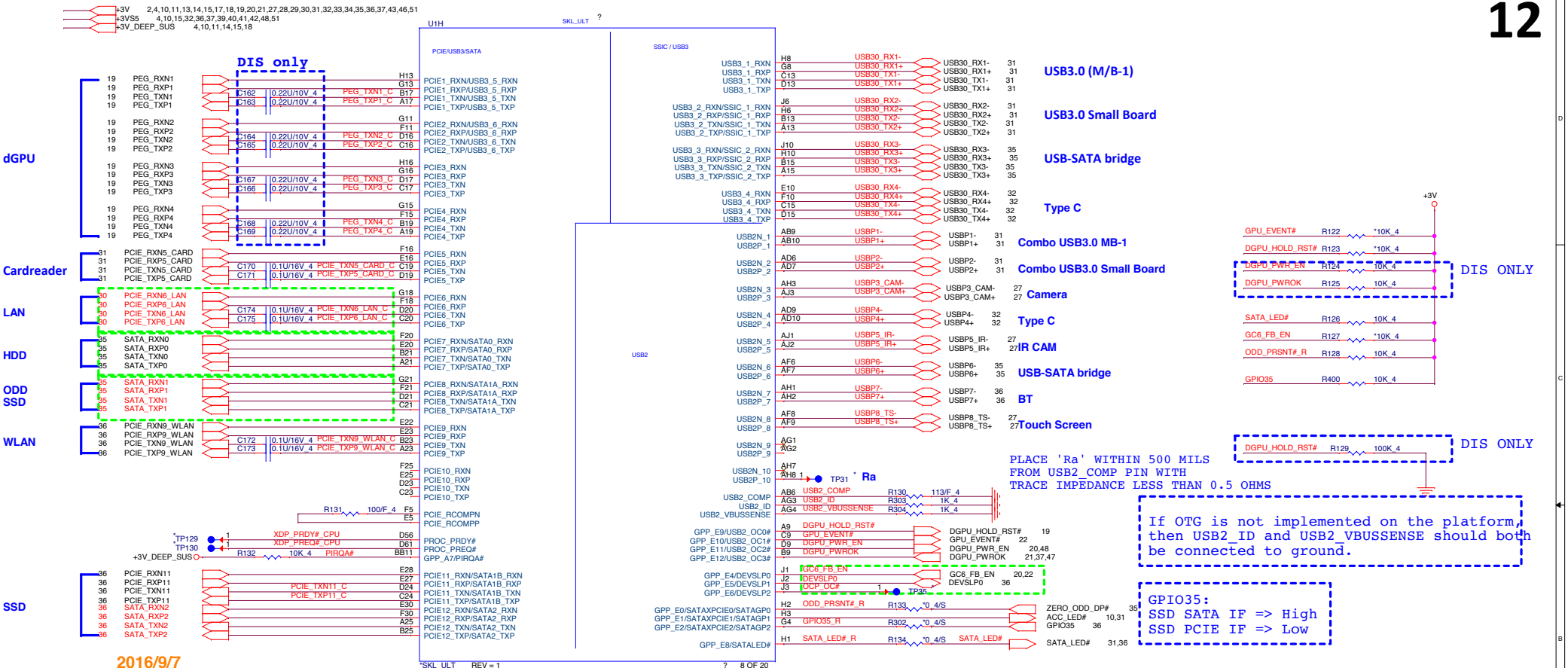

2016/9/7
For Base-U the SATA1B/SATA2 delete

PCI-E Port Mapping Table

PCI-E Port	Function	CLK RQ Port	Function
Port1	dGPU	Port0	VGA
Port2	dGPU	Port1	CR
Port3	dGPU	Port2	SSD
Port4	dGPU	Port3	WLAN
Port5	CardReader	Port4	LAN
Port6	LAN	Port5	Un-used
Port7	HDD		
Port8	SSD		
Port9	WLAN		
Port10	Un-used		
Port11	SSDx2		
Port12	SSDx2/ SATA2		

USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3.0 MB-1
PORT-2	USB3.0 Small Board
PORT-3	USB-SATA bridge
PORT-4	Type C

USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	Cobime USB3.0 MB-1
PORT-2	Cobime USB3.0 Small Board
PORT-3	Camera
PORT-4	Type C
PORT-5	IR CAM
PORT-6	USB-SATA bridge
PORT-7	WLAN
PORT-8	Touch Screen
PORT-9	NC
PORT-10	NC

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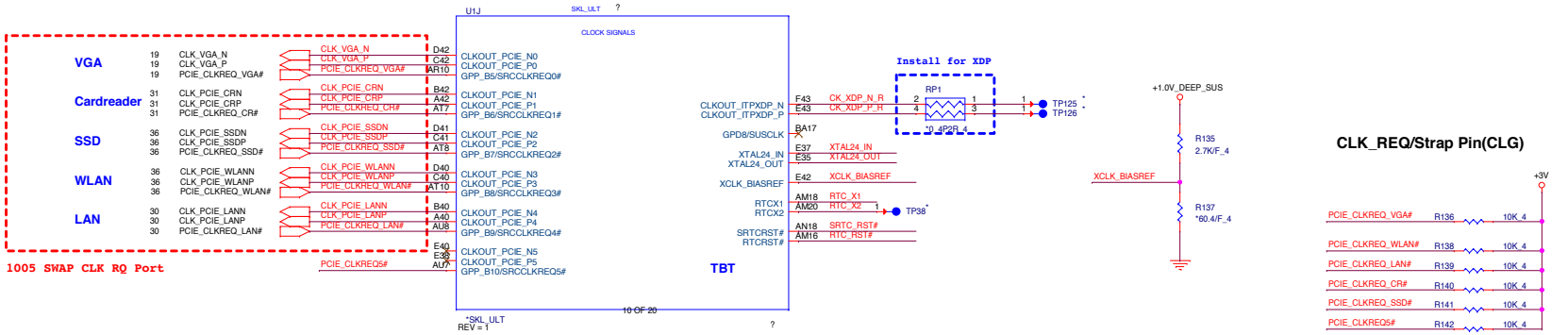
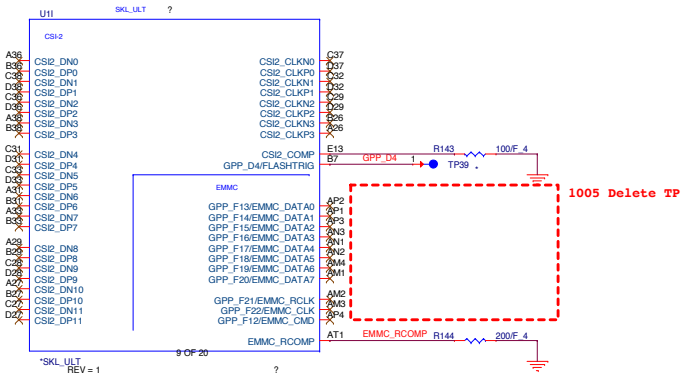
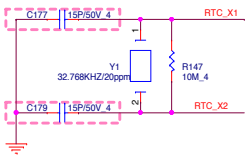
+3V_RTC_2 4,15
+BAT_RTC 4,15,33,38,49
+1.8V_DEEP_SUS 9,15,41
+3V 2,4,10,11,12,14,15,17,18,19,20,21,27,28,29,30,31,32,33,34,35,36,37,43,46,51



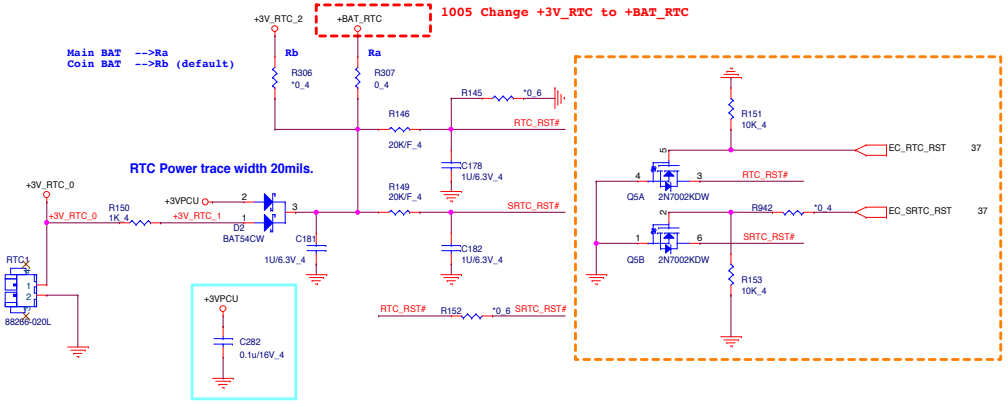


RTC Clock 32.768KHz



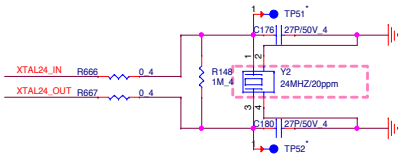
RTC Circuitry(RTC)

30mils



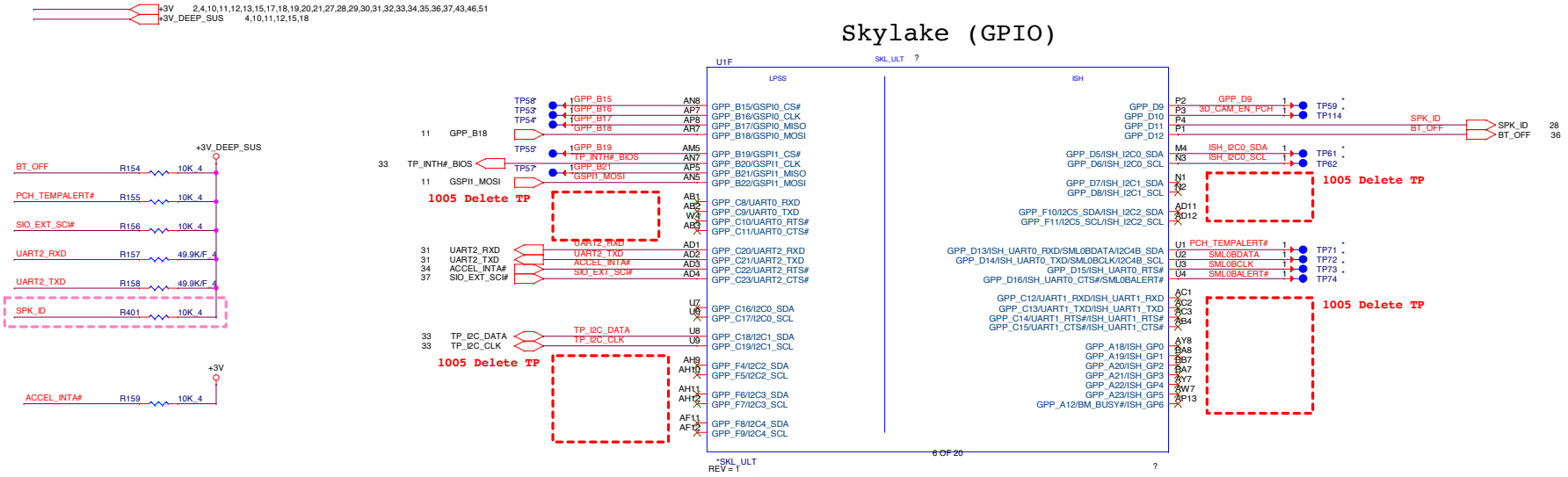
External Crystal

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-U needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-U.

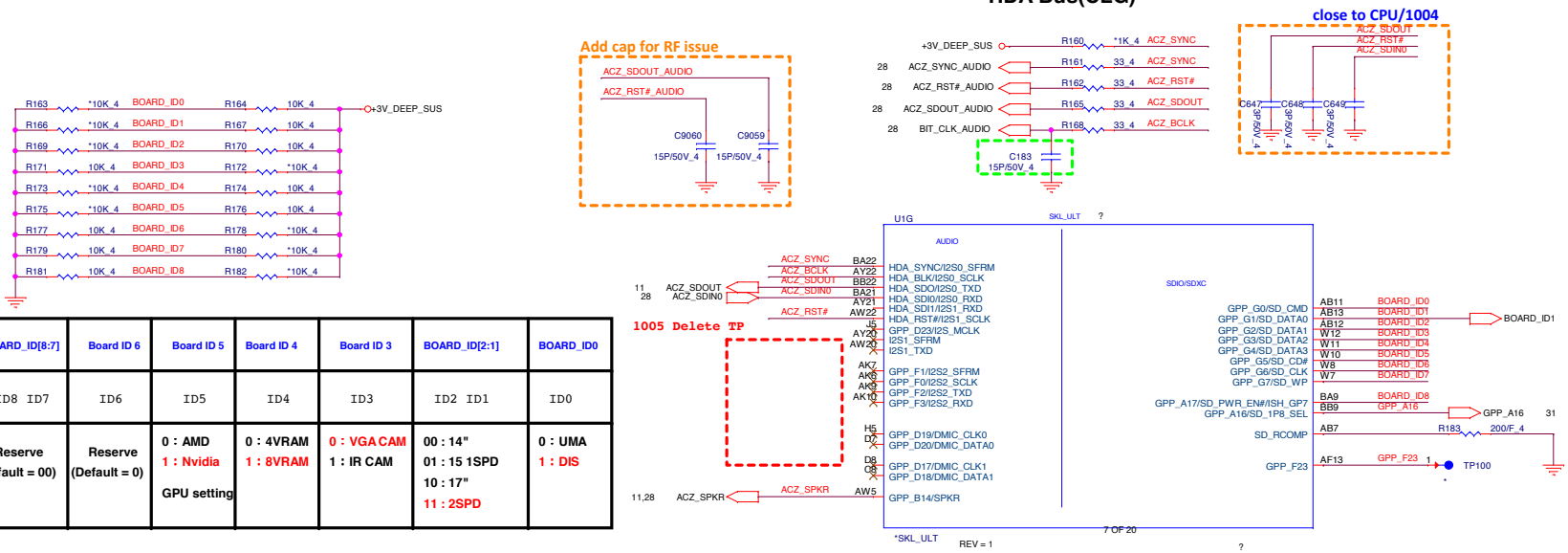


NB5	PROJECT : G74A Quanta Computer Inc.	
Size: Custom	Document Number: 13 -- SKYLAKE 12/15 (CLK/EMMC)	Rev: 1A
Date: Wednesday, January 11, 2017	Sheet 13 of 51	

Skylake (GPIO)



HDA Bus(CLG)



Skylake U	BOARD_ID[8:7]	Board ID 6	Board ID 5	Board ID 4	Board ID 3	BOARD_ID[2:1]	BOARD_ID0
Model	ID8 ID7	ID6	ID5	ID4	ID3	ID2 ID1	ID0
Definition	Reserve (Default = 00)	Reserve (Default = 0)	0 : AMD 1 : Nvidia GPU setting	0 : 4VRAM 1 : 8VRAM	0 : VGA CAM 1 : IR CAM	00 : 14" 01 : 15 1SPD 10 : 17" 11 : 2SPD	0 : UMA 1 : DIS

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Quanta Computer Inc.
NB5
Size: Custom | Document Number: 14 -- SKYLAKE 13/15 (GPIO) | Rev: 1A
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4,10,11,12,14,18 +3V_DEEP_SUS
9,13,41,42 +1.0V_DEEP_SUS
9,41 +1.8V_DEEP_SUS
4,13,33,38,49 +BAT_RTC
4,10,32,36,37,39,40,41,42,48,51 +3VS5

U1O
SKL_ULT
CPU POWER 4 OF 4
15 OF 20
*SKL_ULT
REV = 1

PCH Internal VRM
Ca and Cb close to CPU less then 100 mils
Ca
Cb
close to CPU/1004
close to CPU/1004
for DS3
Main BAT -->Ra
Coin BAT -->Rb (default)
20mils
1005 Change +3V_RTC to +BAT_RTC

2.899A
2.57A
1.714A
0.03A
0.09A

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Quanta Computer Inc.
Size Custom
Document Number 15 -- SKYLAKE 14/15(PCH POWER)
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NB5

NB5

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Quanta Computer Inc.

Size	Document Number	Rev
	16 -- SKYLAKE 15/15 XDP&APS *	1A

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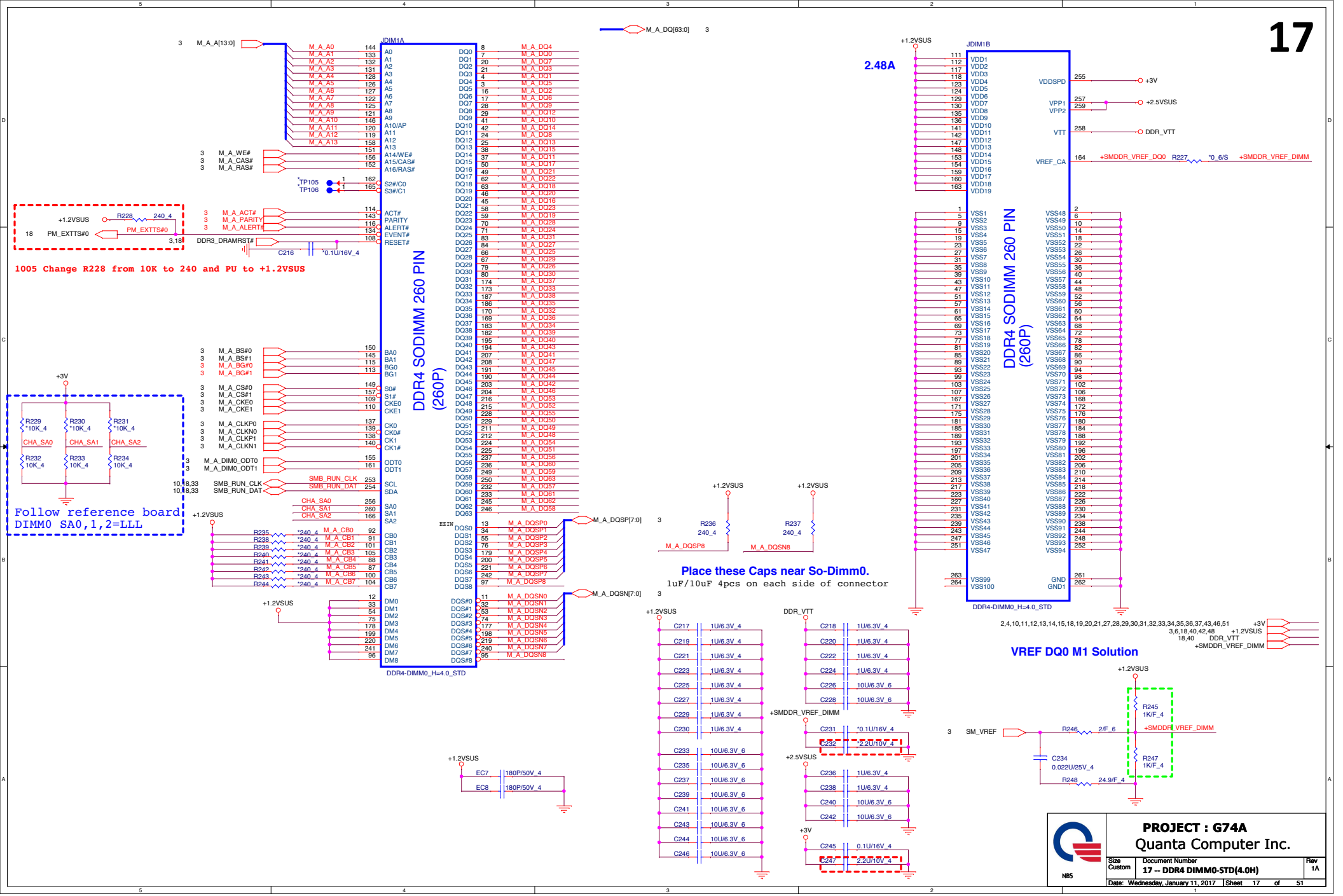
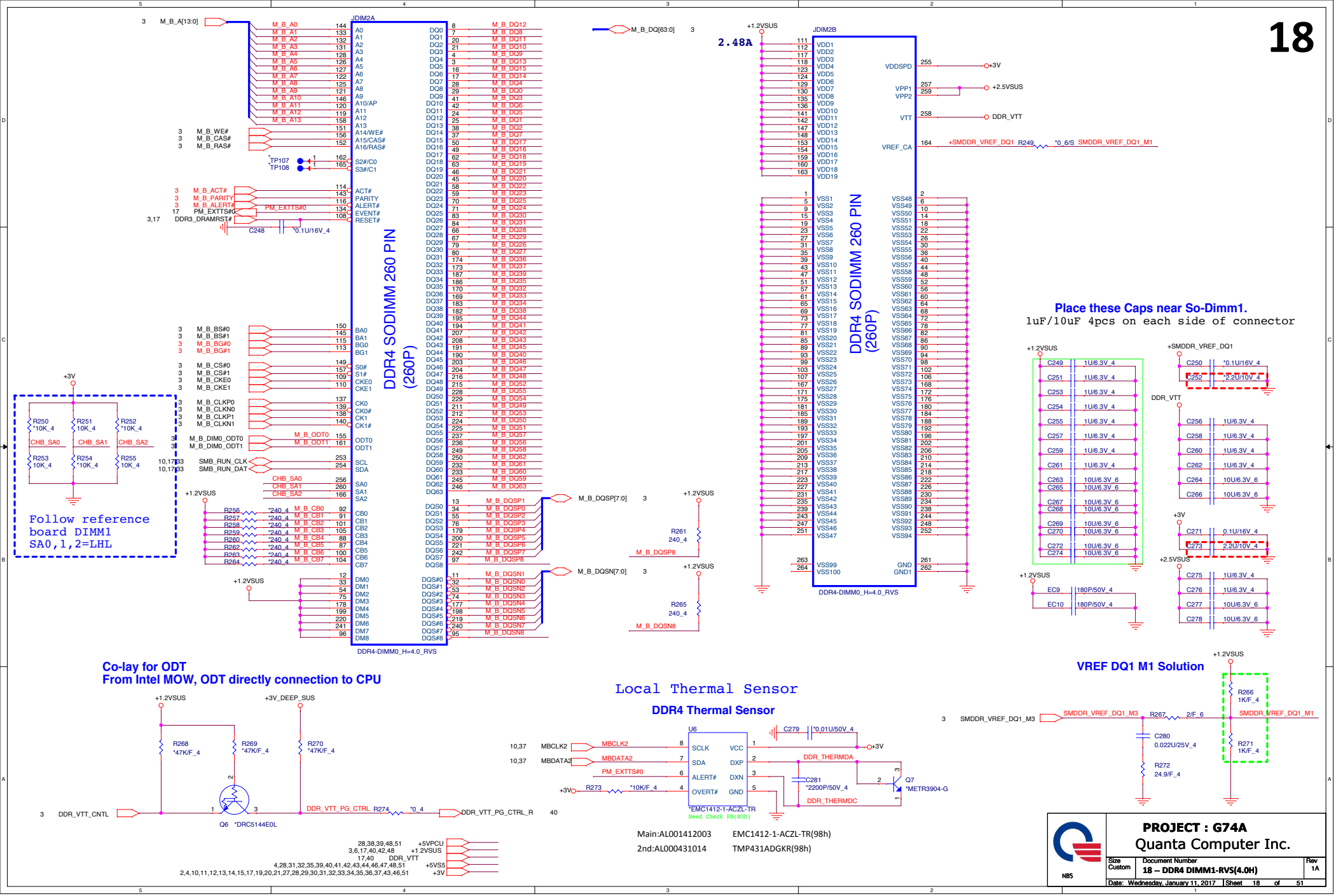

JDIM1A
DDR4 SODIMM 260 PIN (260P)
DDR4-DIMM0_H=4.0_STD
JDIM1B
DDR4 SODIMM 260 PIN (260P)
DDR4-DIMM0_H=4.0_STD
2.48A
1005 Change R228 from 10K to 240 and PU to +1.2VSUS
Follow reference board DIMM0 SA0,1,2=LLL
Place these Caps near So-Dimm0.
1uF/10uF 4pcs on each side of connector
VREF DQ0 M1 Solution
M_A_DQ[63:0]
M_A_DQSP[7:0]
M_A_DQSN[7:0]
+1.2VSUS
+3V
+2.5VSUS
DDR_VTT
+SMDDR_VREF_DIMM



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Quanta Computer Inc.	
Size: Custom	Document Number: 18 -- DDR4 DIMM1-RVS(4.0H)
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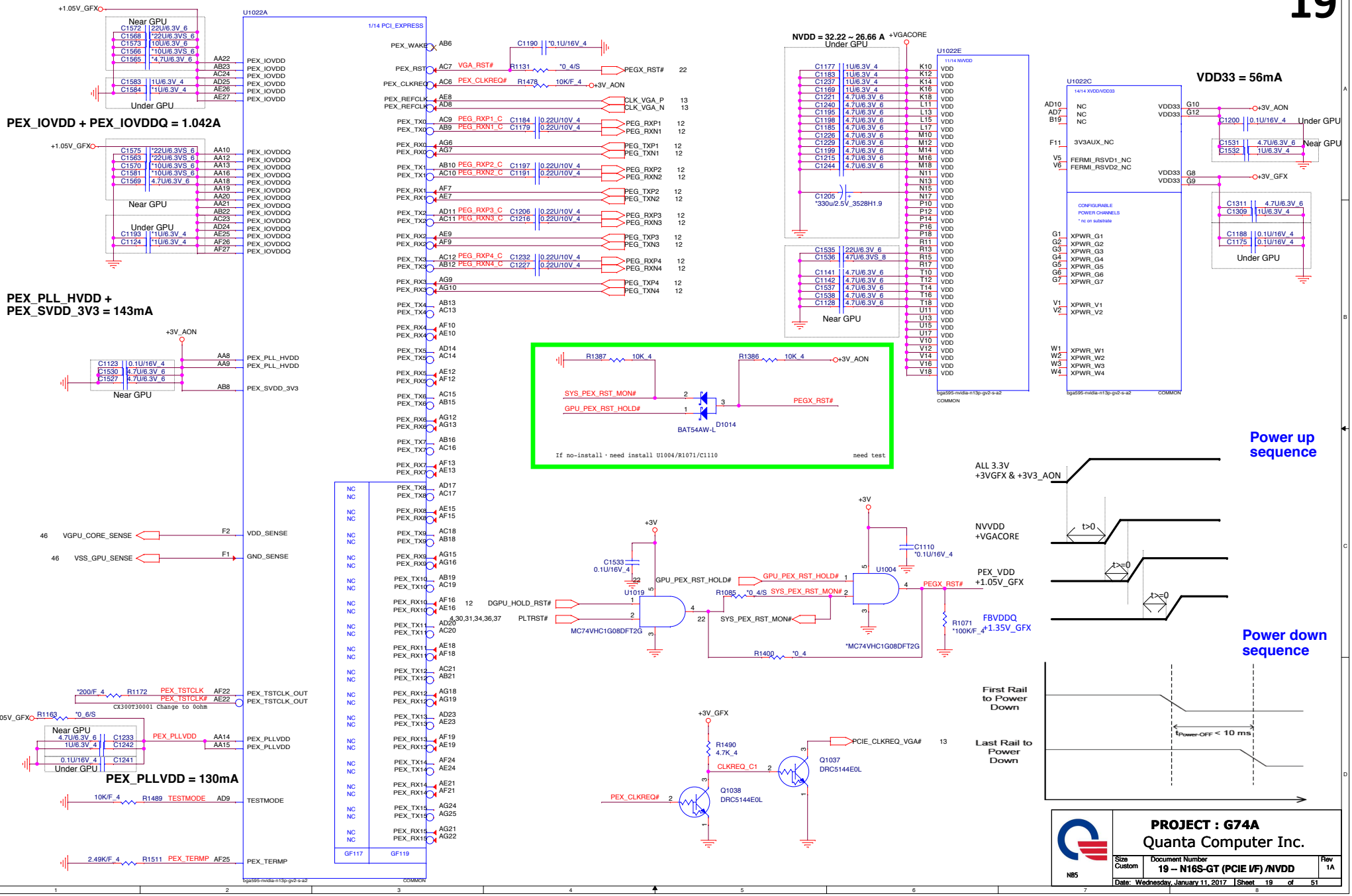

PROJECT : G74A	
Quanta Computer Inc.	
Size: Custom	Document Number: 19 – N16S-GT (PCIE I/F) /NVDD
Rev: 1A	
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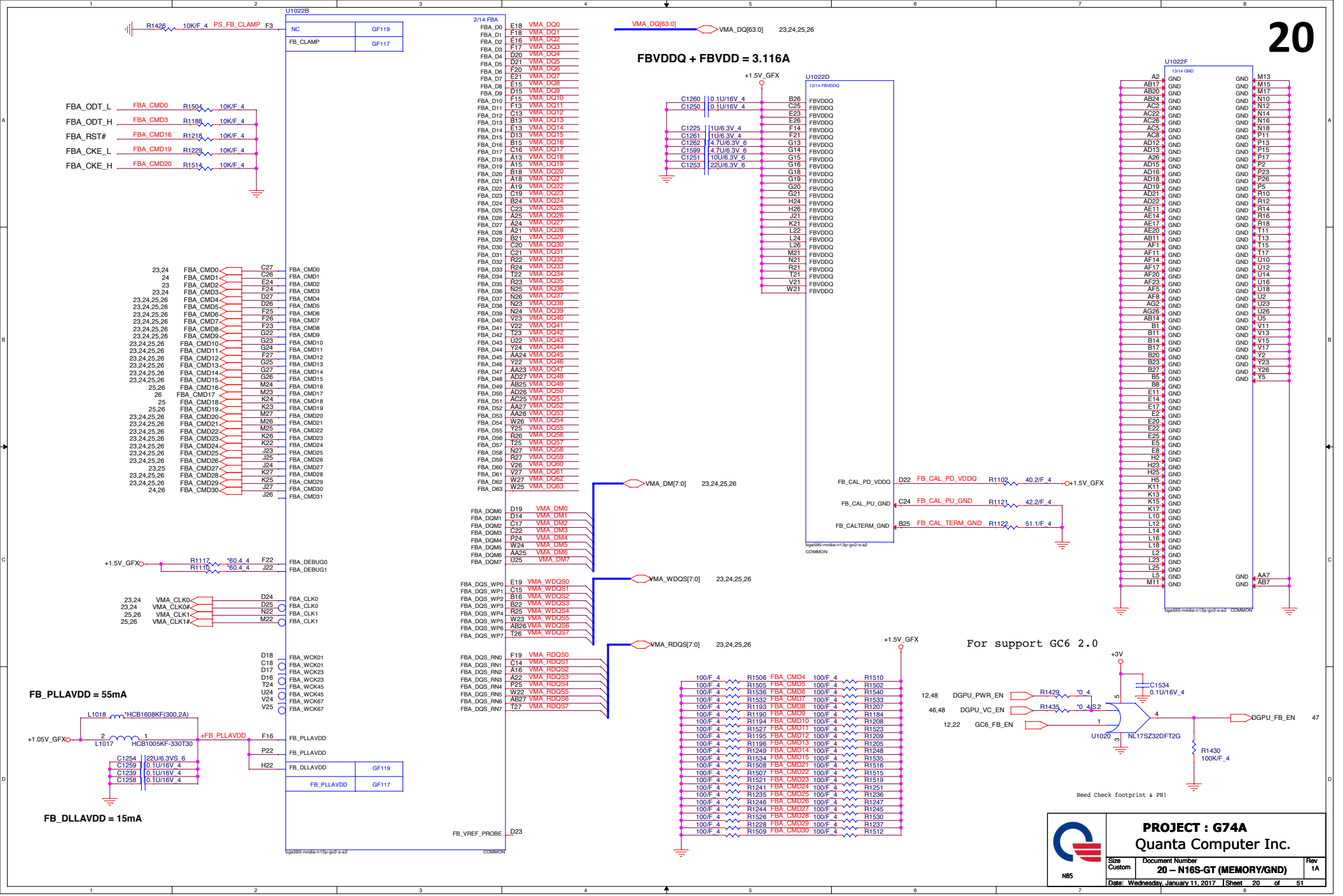
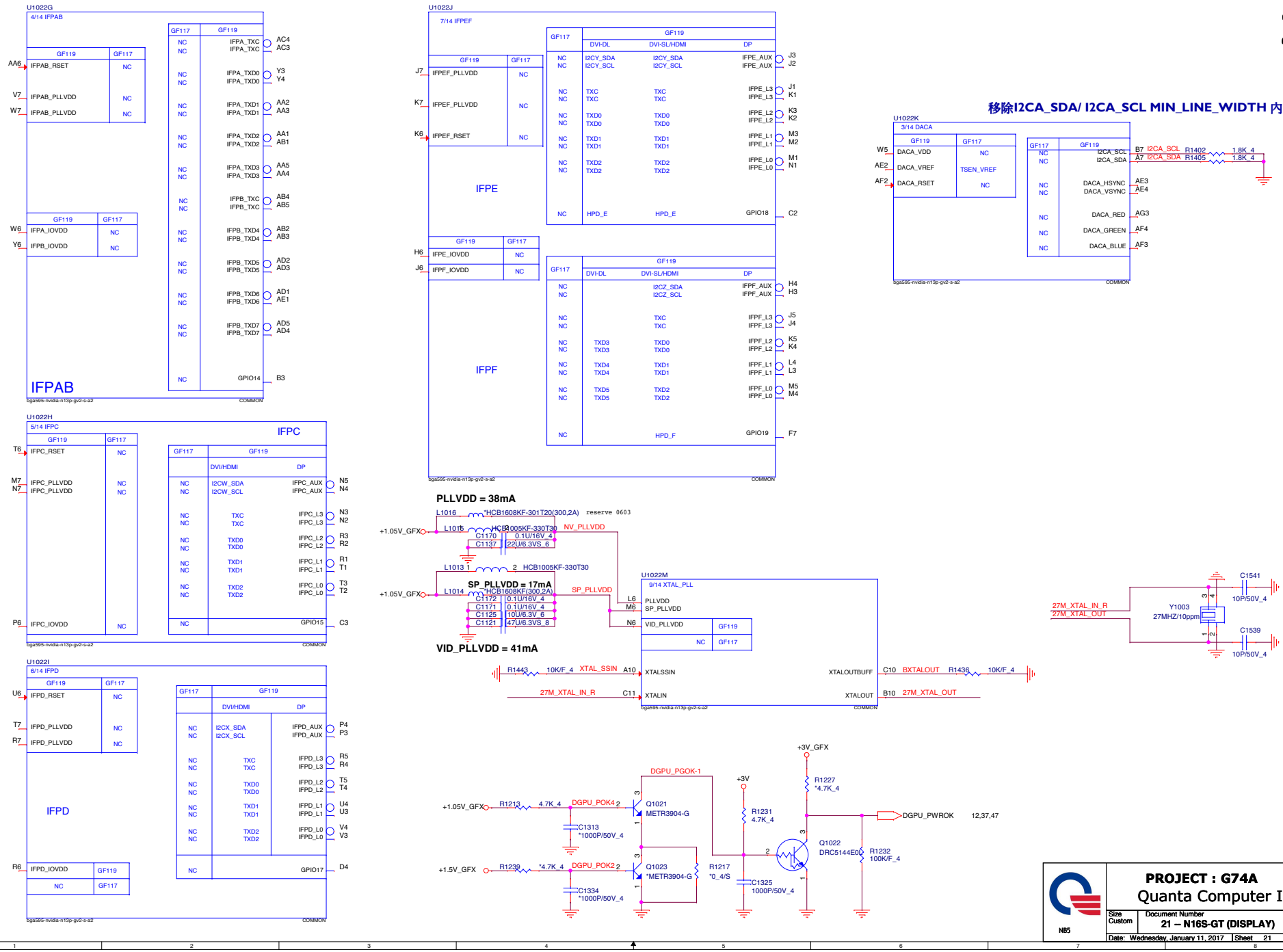
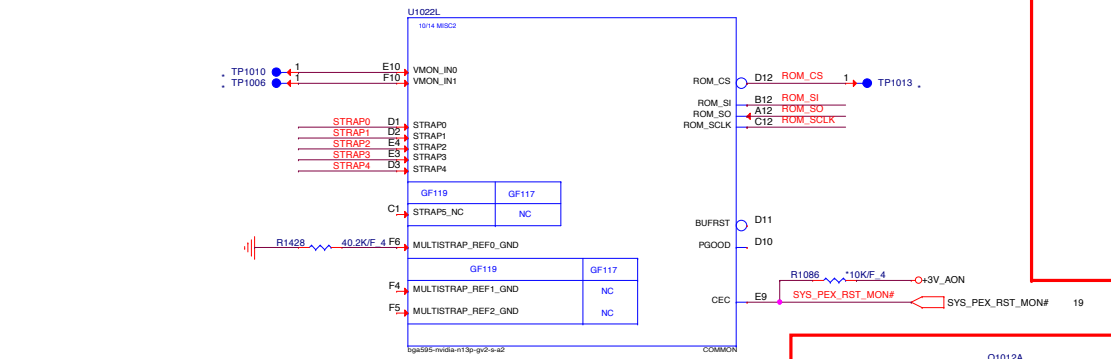
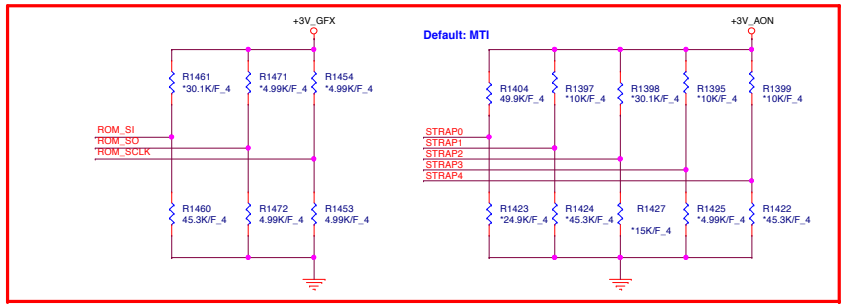


移除I2CA_SDA/ I2CA_SCL MIN_LINE_WIDTH 內的數值.

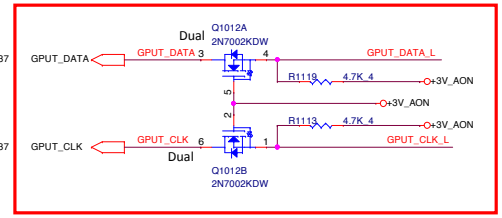


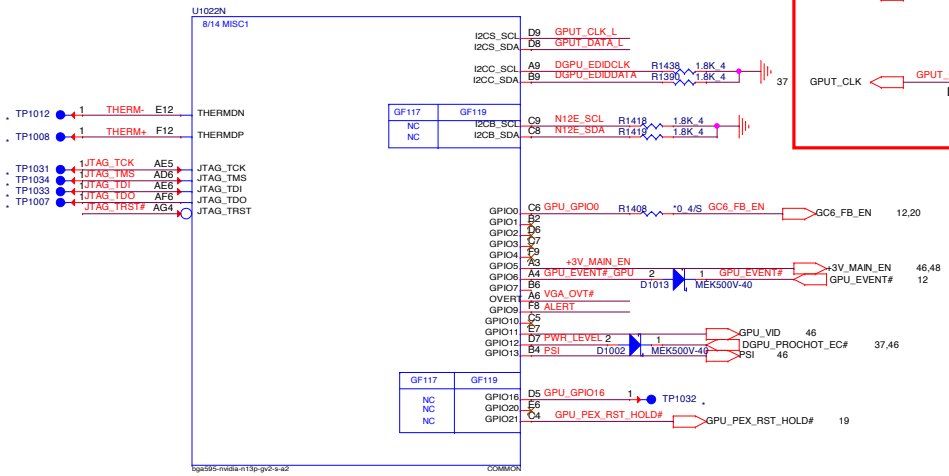




22

4.99k	CS24992FB26
10k	CS31002FB26
15k	CS31502FB24
20k	CS32002FB29
24.9k	CS32492FB16
30.1k	CS33012FB18
34.8k	CS33482FB22
45.3k	CS34532FB18





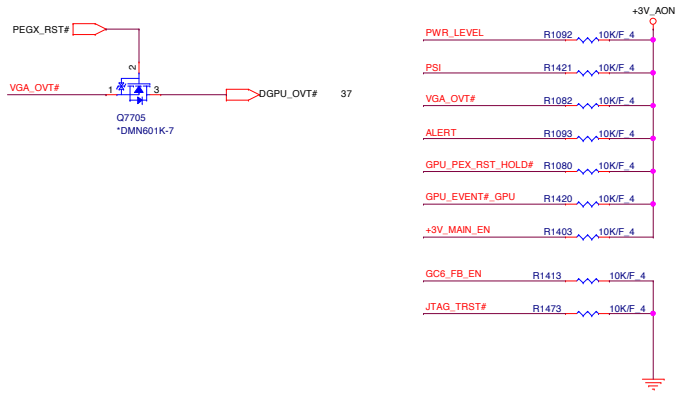


Table 15-2. Resistance Mapping to Hex Values

Resistor Values	Pull-Up to 3V3_MAIN	Pull-Down to GND
4.99 kΩ	1000	0000
10.0 kΩ	1001	0001
15.0 kΩ	1010	0010
20.0 kΩ	1011	0011
24.9 kΩ	1100	0100
30.1 kΩ	1101	0101
34.8 kΩ	1110	0110
45.3 kΩ	1111	0111

VRAM Configuration Table

ROM_SI E

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	256Mx16 Strap	128Mx16 Strap	QBC	TOP B/S
1100	DDR3 256Mx16, 64bit, 4Gb,1GMHz	HYNIX	H5TC4G63CFR-N0C	0XC	0x9	AKD5PZDTW02	AKD5PZDTW01
0111	DDR3 256Mx16, 64bit, 4Gb,1GMHz	Micron	MT41J256M16LY-091G:N	0x7	0x3	AKD59GSTL01	AKD59GSTL00
1111	DDR3 256Mx16, 64bit, 4Gb,1GMHz	SAMSUNG	K4W4G1646E-BC1A	0XD	0x4	AKD5PGDT501	AKD5PGDT500

GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor
1	OUT	MEM_VDD_CTL	Memory VDD VID
2	OUT	LCD_BL_PWM	Panel Backlight PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	Reserved	--
6	OUT	FB_CLAMP_TGL_REQ	Active low FB Clamp toggle request
7	OUT	3D VISION	3D VISION LEFT/RIGHT signal
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM VREF_CTL	MEMMORY VREF CONTROL
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

R9066 *1K_4
R9067 *1K_4
R9068 *1K_4
R9069 *1K_4

NB5

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Rank0

HYU 256Mx16, H5TC4G63AFR-11C QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07
MIC 256Mx16, MT41J256M16HA-093G:E QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
SAM 256Mx16, K4W4G1646D-BC1A QBC PN : AKD5PGWT501---TOP B/S PN : AKD5PGWT502

U1021

VRAM _DDR3_MTI_256MX16

U1024

VRAM _DDR3_MTI_256MX16

162_1% ohm CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
CS11622FB15 RES CHIP 162 1/16W +-1%(0402)

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Quanta Computer Inc.	
Size: Custom	Document Number: 23 -- VRAM DDR3L - RANK0
Rev: 1A	
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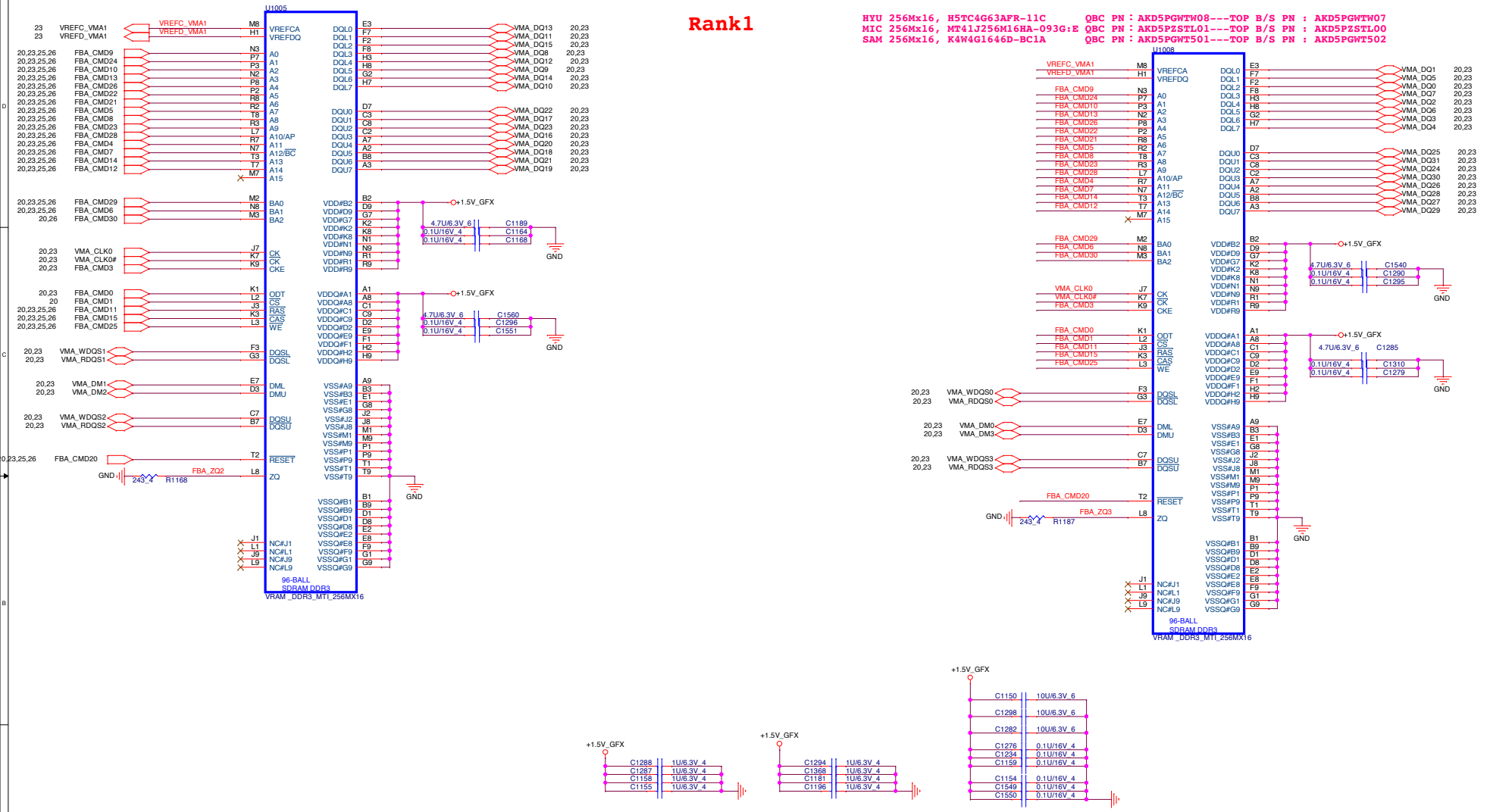
NB5	

Rank1

HYU 256Mx16, H5TC4G63AFR-11C QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07
MIC 256Mx16, MT41J256M16HA-093G:E QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
SAM 256Mx16, K4W4G1646D-BC1A QBC PN : AKD5PGWT501---TOP B/S PN : AKD5PGWT502



NB5	PROJECT : G74A Quanta Computer Inc.	
Size: Custom	Document Number: 24 -- VRAM DDR3L - RANK1	Rev: 1A
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Rank0

HYU 256Mx16, H5TC4G63AFR-11C
MIC 256Mx16, MT41J256M16HA-093G:E
SAM 256Mx16, K4W4G1646D-BC1A

QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07
QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
QBC PN : AKD5PGWT501---TOP B/S PN : AKD5PGWT502

U1026

VRAM _DDR3_MT1_256MX16

162_1% ohm CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
CS11622FB15 RES CHIP 162 1/16W +-1%(0402)

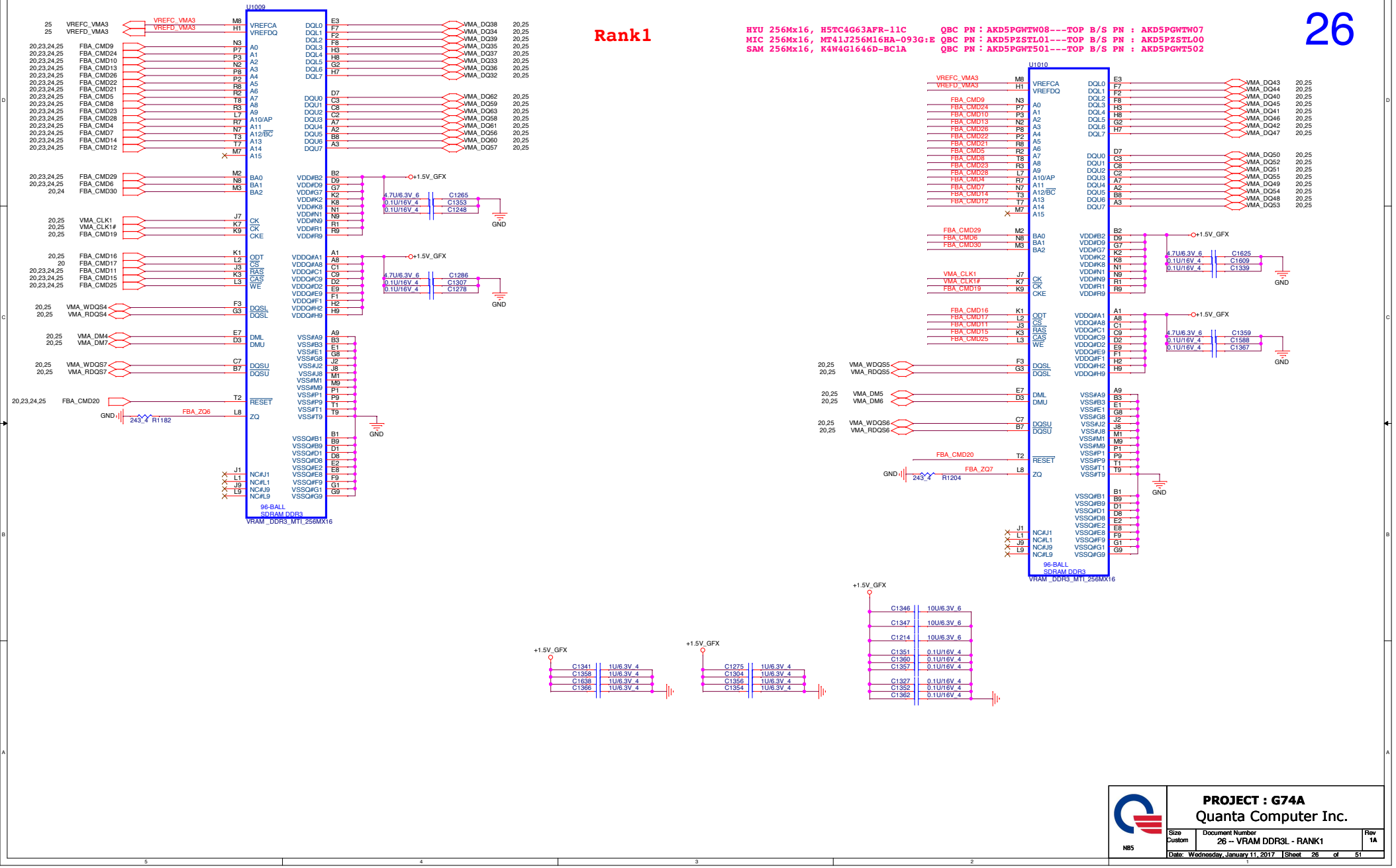
U1027

VRAM _DDR3_MT1_256MX16

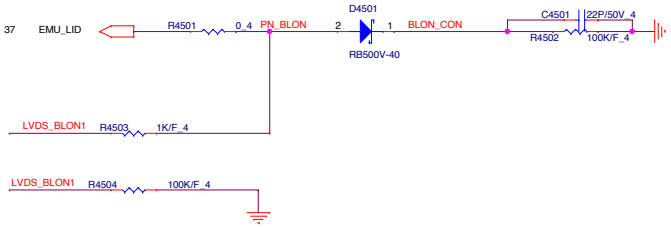
FOR EMI Request

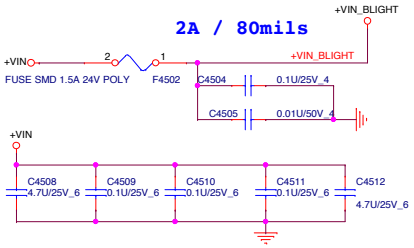
Rank1

HYU 256Mx16, H5TC4G63AFR-11C QBC PN : AKD5PGWTW08---TOP B/S PN : AKD5PGWTW07
MIC 256Mx16, MT41J256M16HA-093G:E QBC PN : AKD5PZSTL01---TOP B/S PN : AKD5PZSTL00
SAM 256Mx16, K4W4G1646D-BC1A QBC PN : AKD5PGWT501---TOP B/S PN : AKD5PGWT502

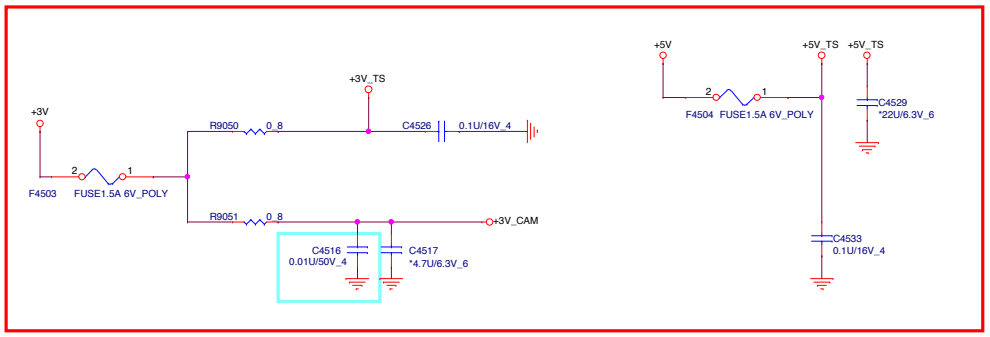


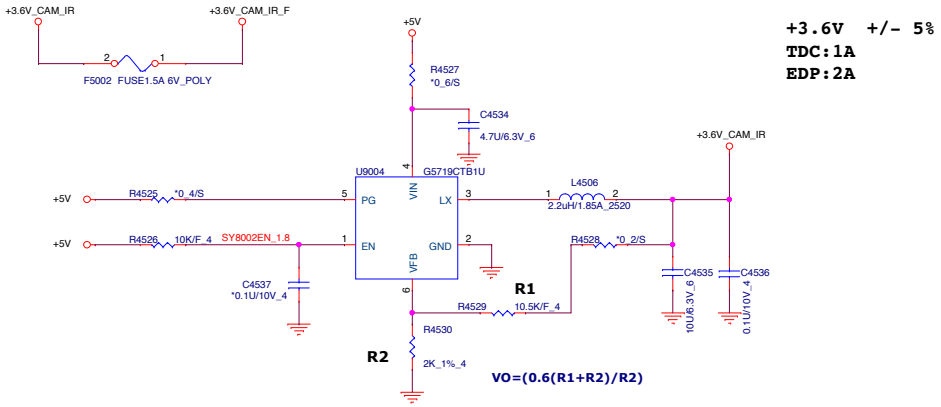
LID Switch





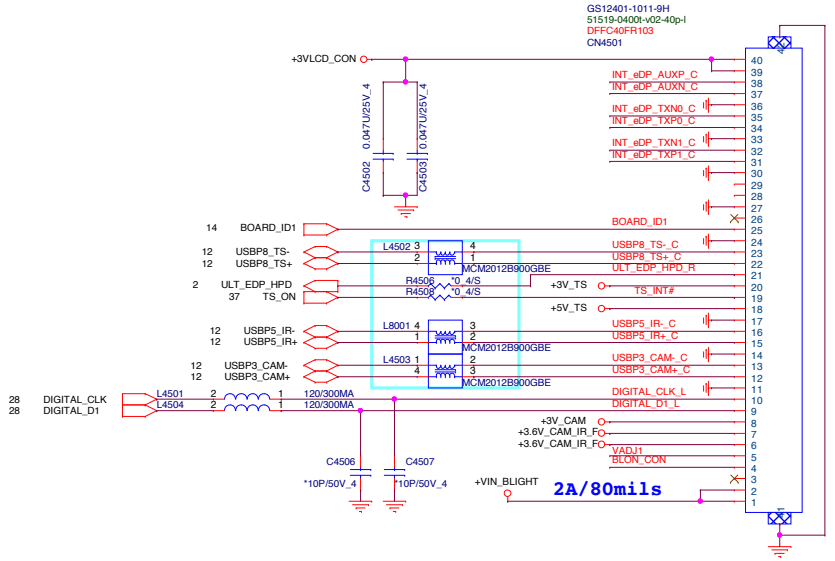
Touch screen

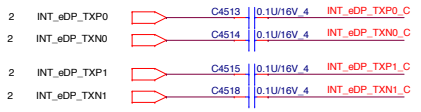


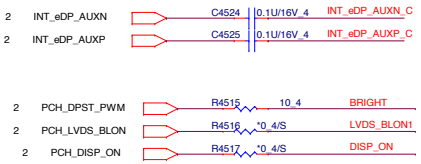


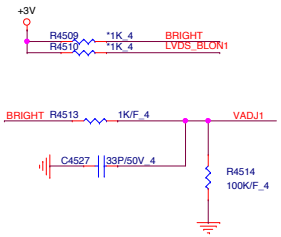
+3.6V +/- 5%
TDC:1A
EDP:2A

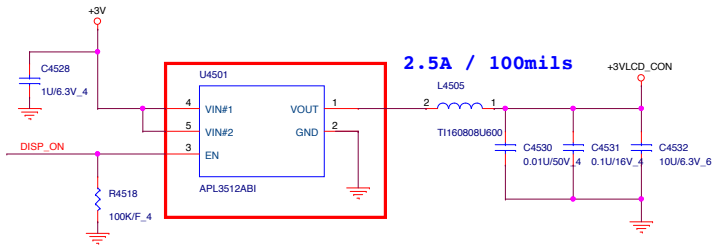
eDP Conn.

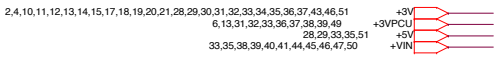












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Quanta Computer Inc.	
Size: Custom	Document Number: 27 -- eDP CONN/LID/CAM/D-MIC/TS
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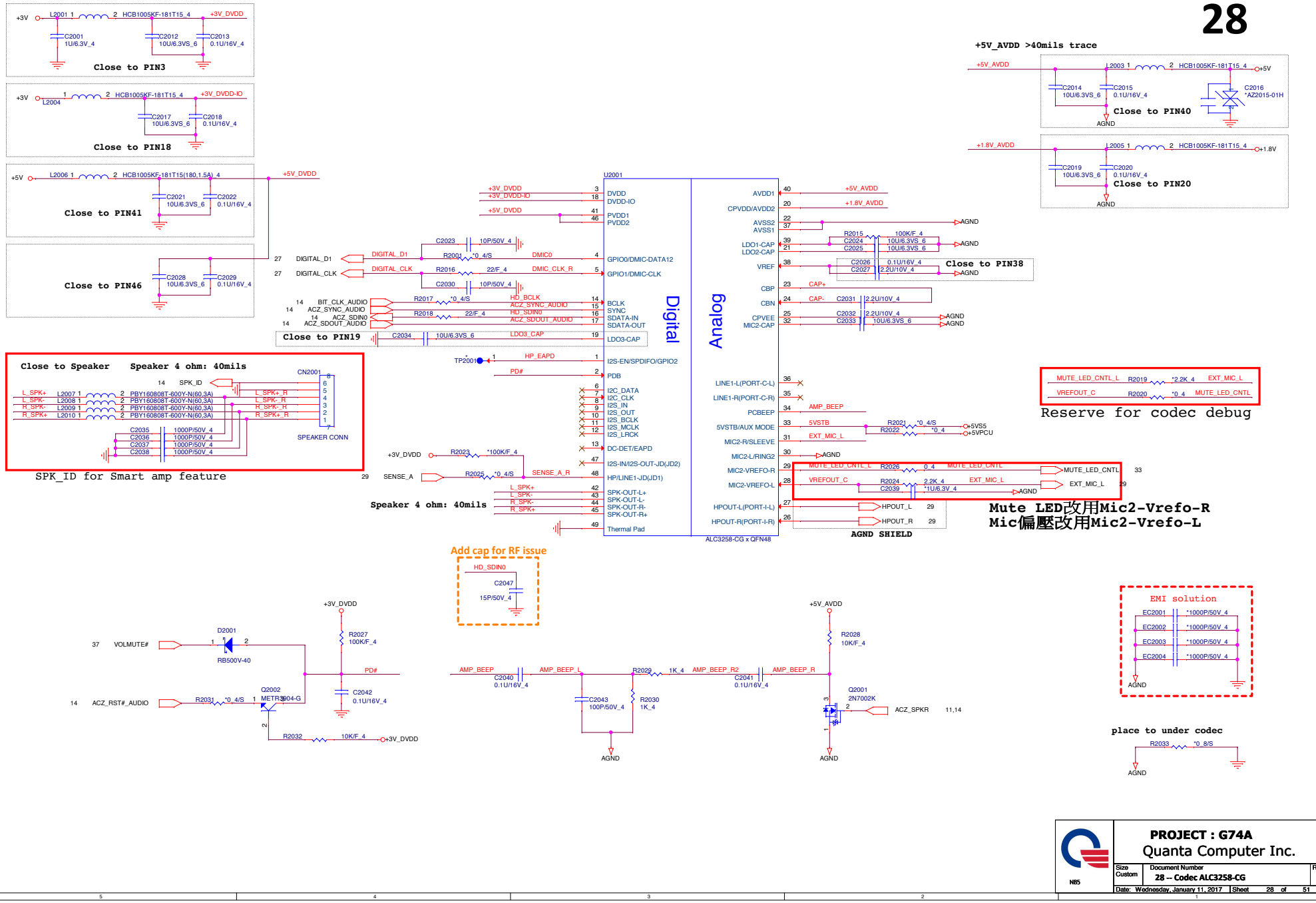

PROJECT : G74A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	28 -- Codec ALC3258-CG	1A

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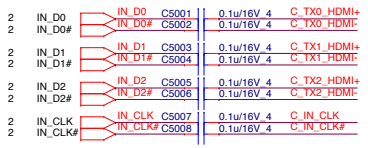
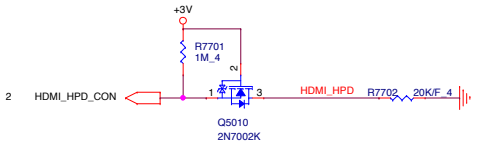
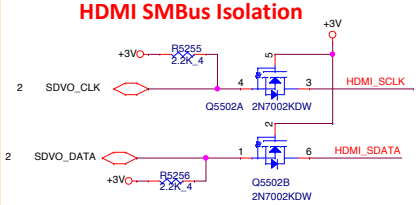
HDMI CONN

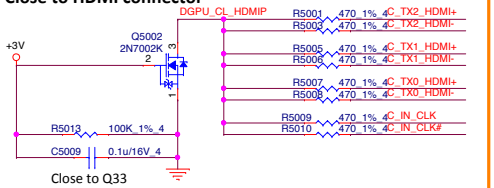




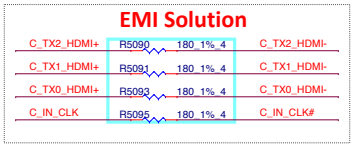
HDMI SMBus Isolation

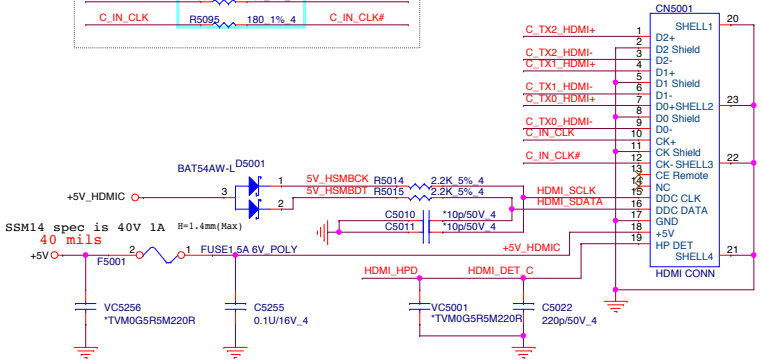


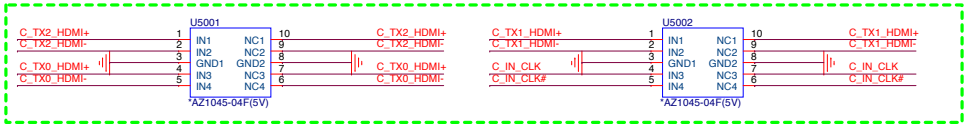
Close to HDMI connector



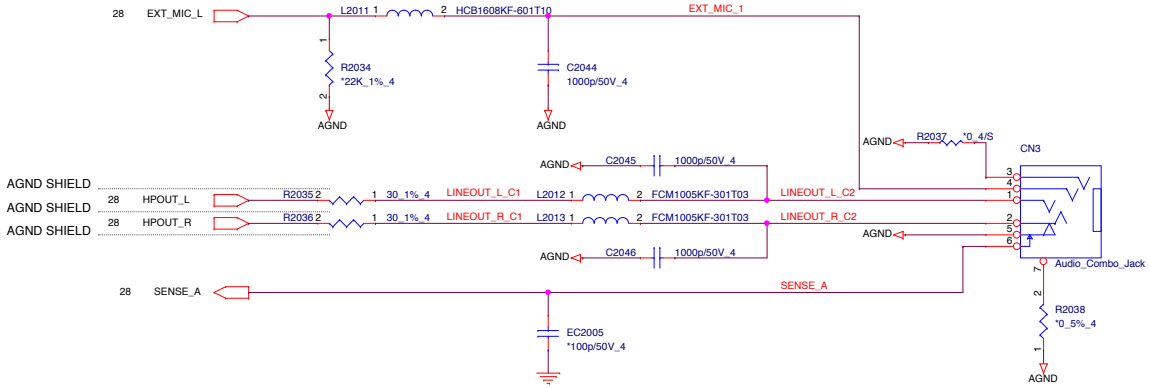
EMI Solution



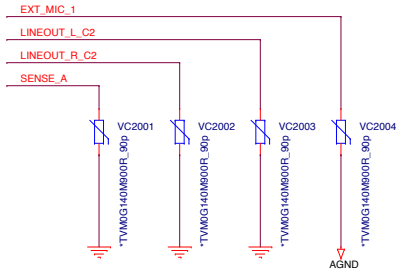




Audio Jack



Audio JACK ESD



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Quanta Computer Inc.
Size: Custom
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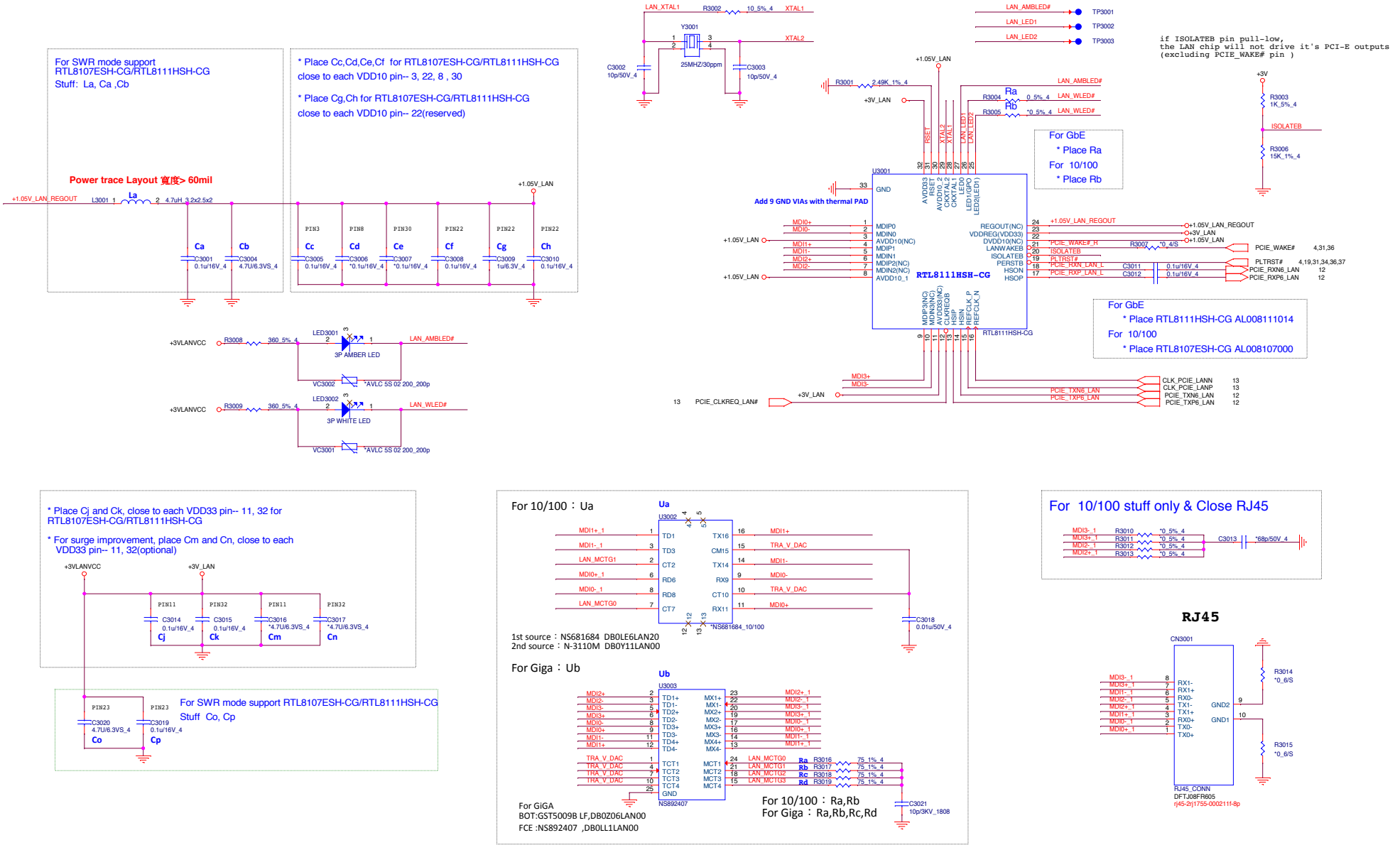
LAN RTL8107ESH-CG/RTL8111HSH-CG



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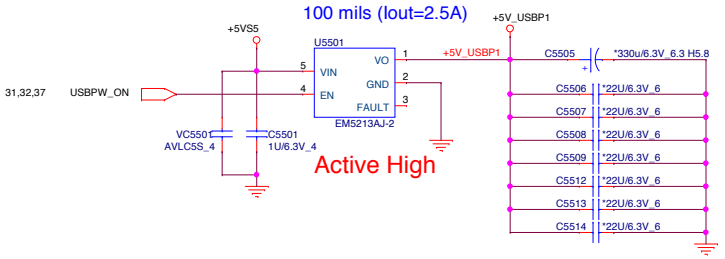
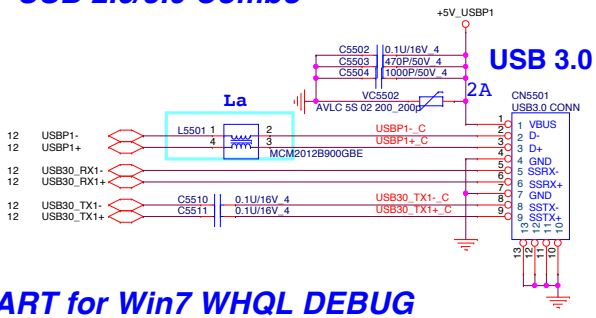
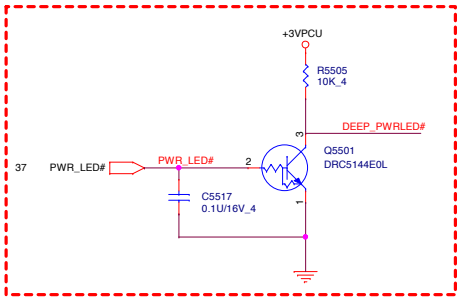


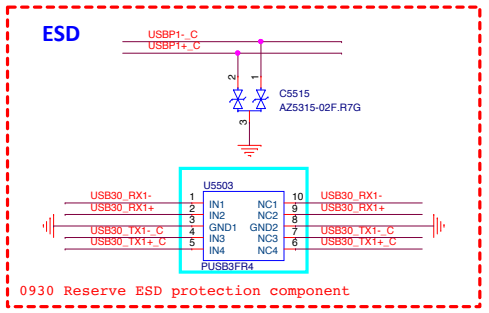
USB 2.0/3.0 Combo



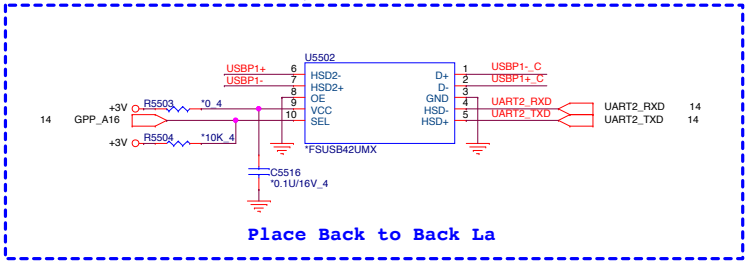
Daughter Board

1123 Add PWR LED MOS Circuit



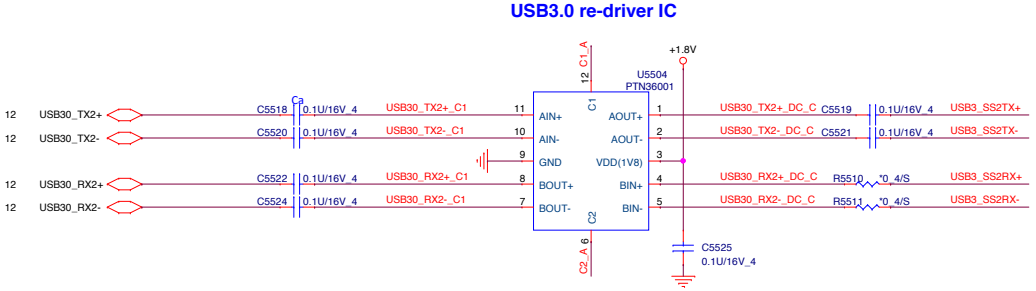


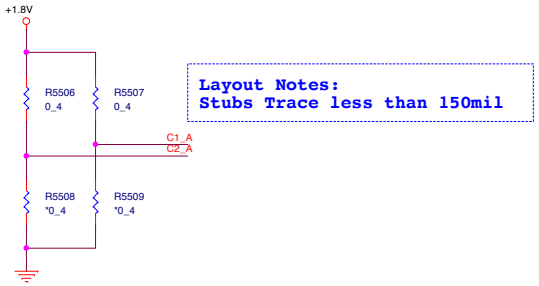
UART for Win7 WHQL DEBUG

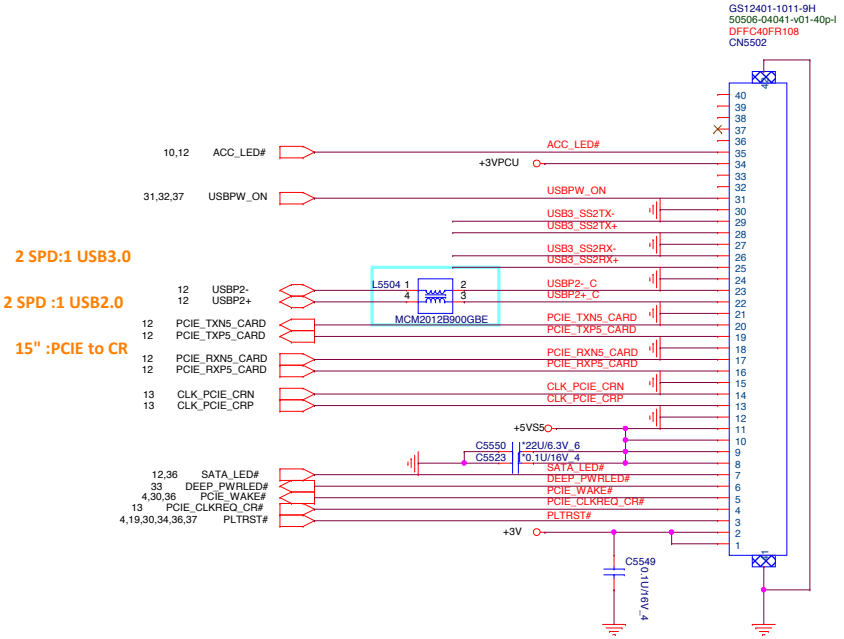


USB3.0

USB3.0 Re-driver IC







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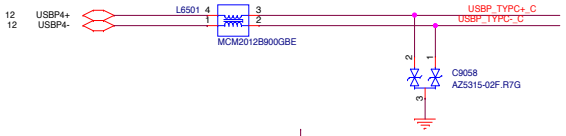
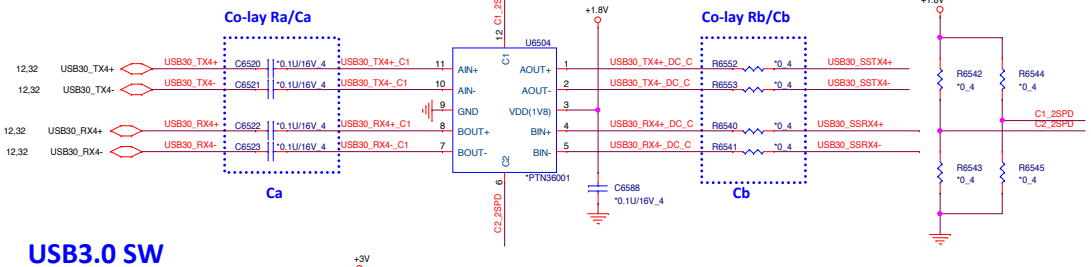
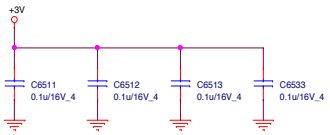
USB3 SW - EJ179S + USB TYPE-C - TPS25810

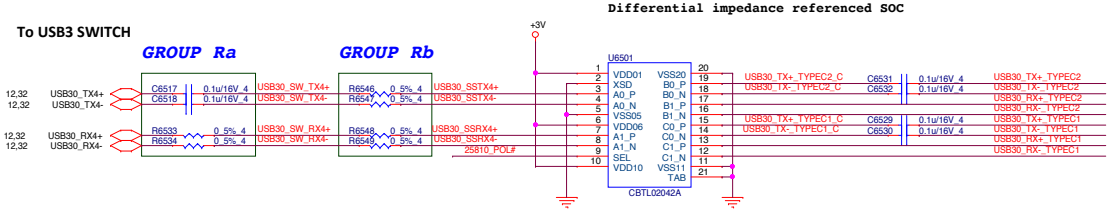
USB2.0

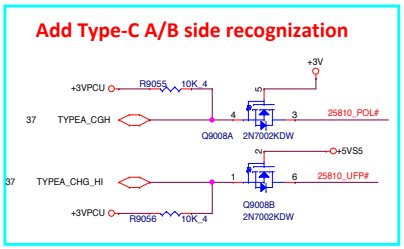




USB3.0 SW

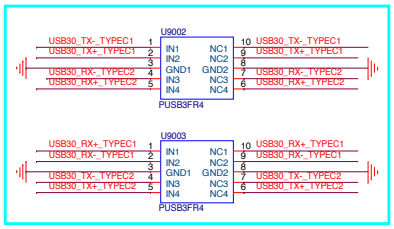


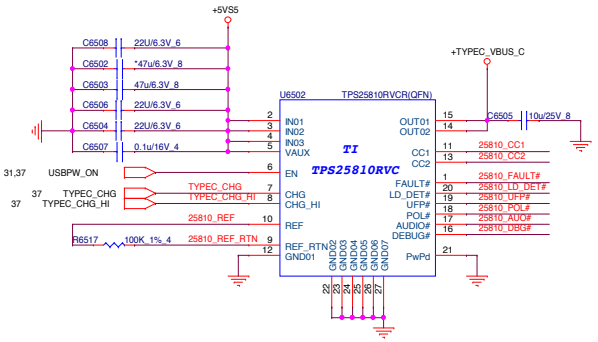


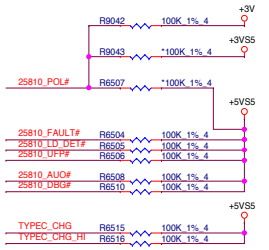


SEL = CMOS single-ended input
operation mode select
SEL = LOW: A <---> B
SEL = HIGH: A <---> C

TYPE C USB3.0 ESD

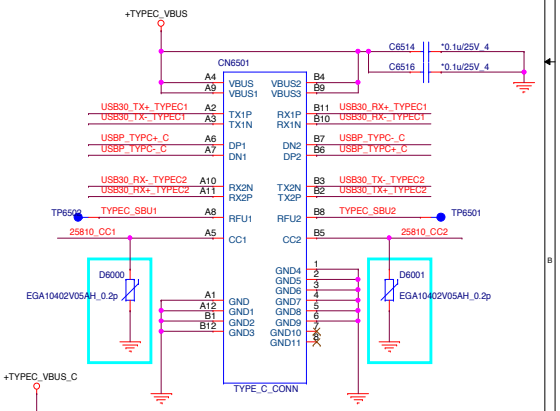


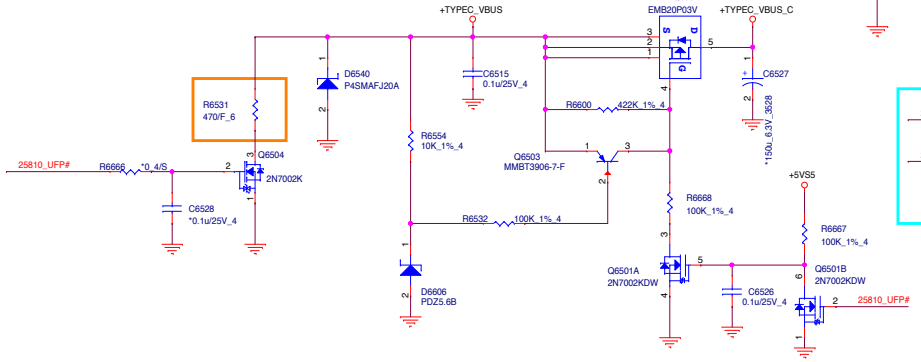




TPS25810 Port	CC1	CC2	TPS25810 Response					
			OUT	VCONN On CC1 or CC2	POLb	UFPb	AUDIOb	DEBUGb
Nothing Attached	OPEN	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
UFP Connected	Rd	OPEN	IN1	NO	Hi-Z	LOW	Hi-Z	Hi-Z
UFP Connected	OPEN	Rd	IN1	NO	LOW	LOW	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	OPEN	Ra	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/No UFP Connected	Ra	OPEN	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Rd	Ra	IN1	CC2	Hi-Z	LOW	Hi-Z	Hi-Z
Powered Cable/UFP Connected	Ra	Rd	IN1	CC1	LOW	LOW	Hi-Z	Hi-Z
Debug Accessory Connected	Rd	Rd	OPEN	NO	Hi-Z	Hi-Z	Hi-Z	LOW
Audio Adapter Accessory Connected	Ra	Ra	OPEN	NO	Hi-Z	Hi-Z	LOW	Hi-Z

CHG	CHG_HI	CC Capability Broadcast	Current Limit	Load Detect Threshold
0	0	STD	1.67 A	NA
0	1	STD	1.67 A	NA
1	0	1.5 A	1.67 A	NA
1	1	3.0 A	3.34 A	1.77 A





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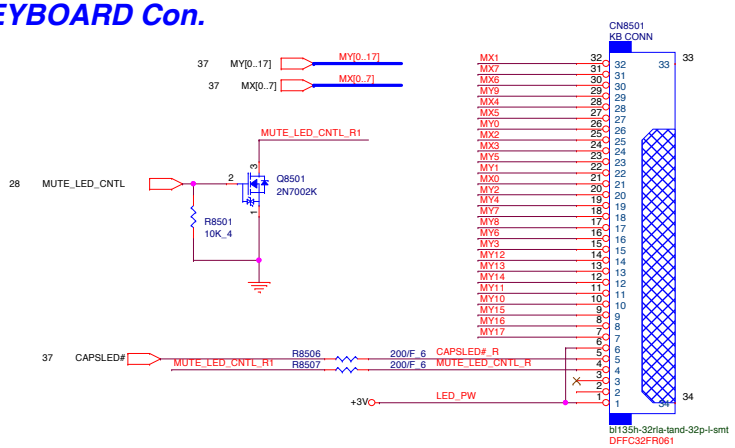
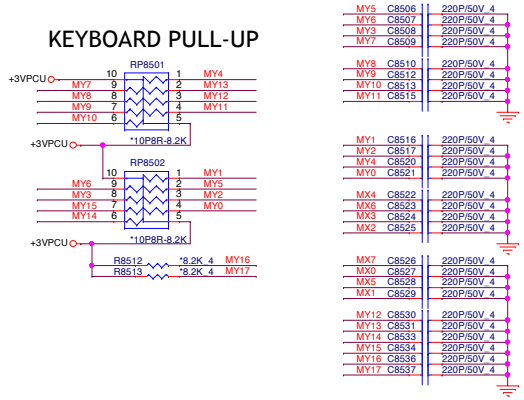
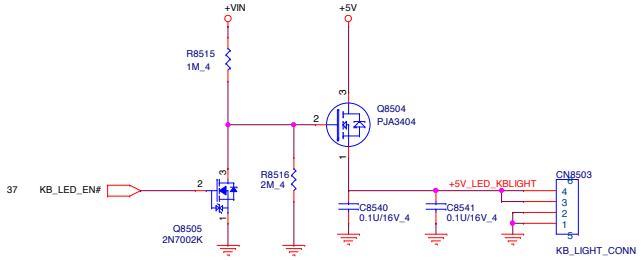
KEYBOARD Con.



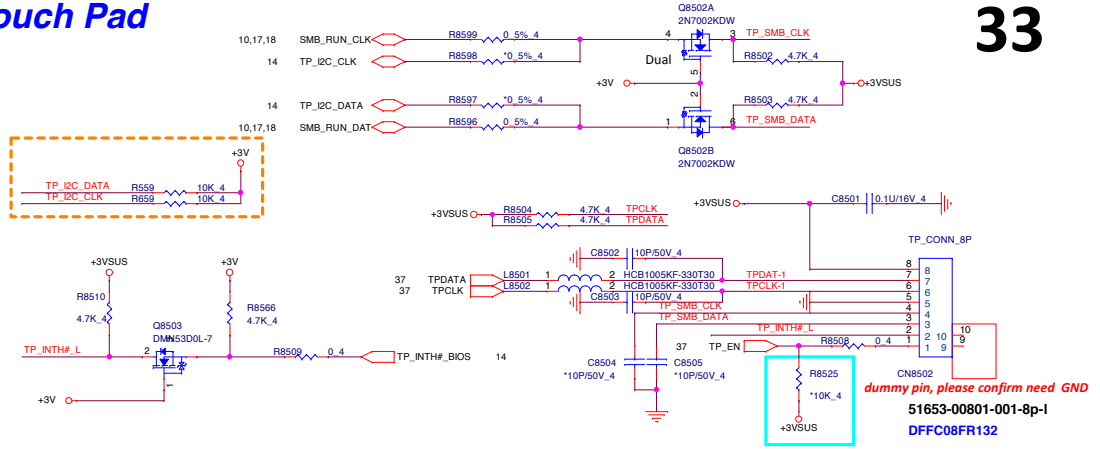
KEYBOARD PULL-UP



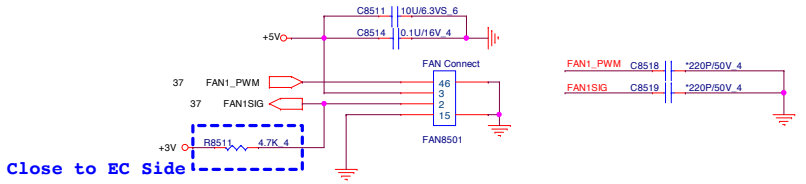
KB LIGHT CONN



Touch Pad

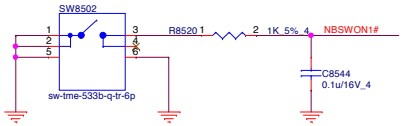


FAN

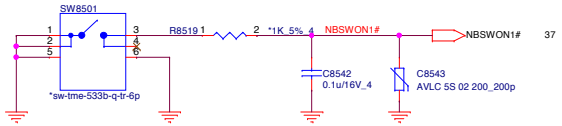


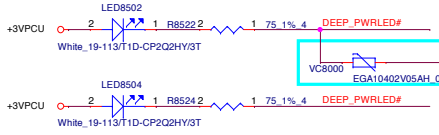
PWR Button & LED & HALL IC

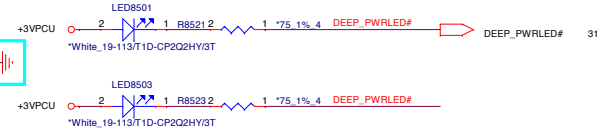
15.6" SW & LED



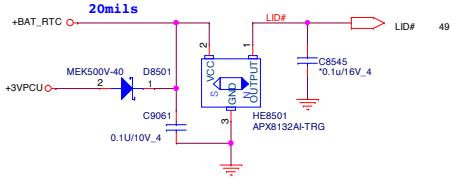
17.3" SW & LED



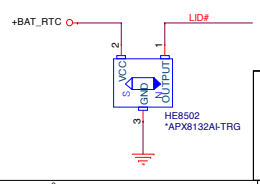




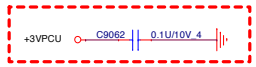
15.6" Hall sensor



17.3" Hall sensor



1024/add C9062 for EMI request



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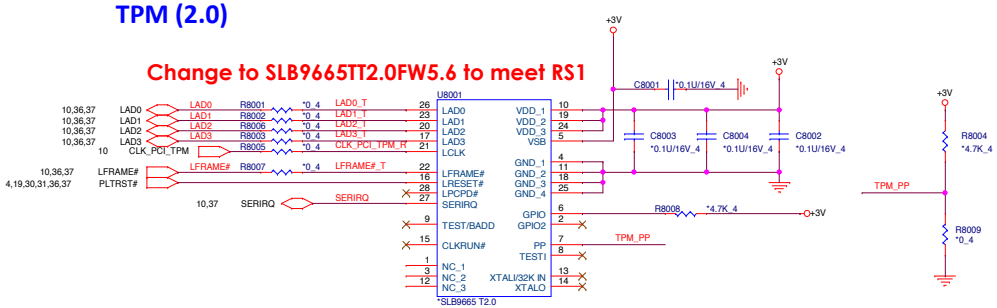
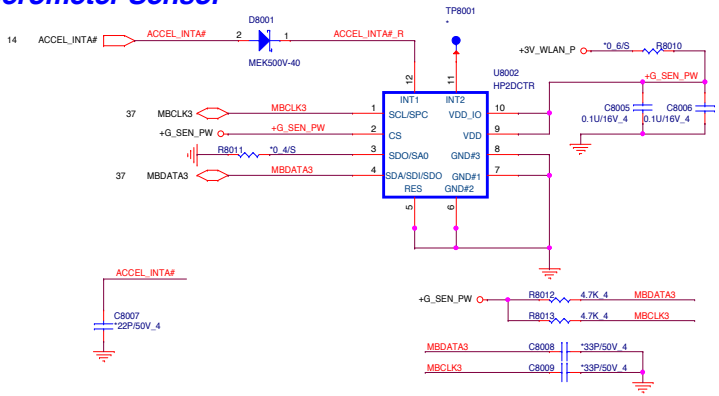
TPM (2.0)

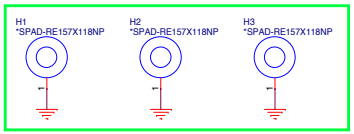
Change to SLB9665TT2.0FW5.6 to meet RS1



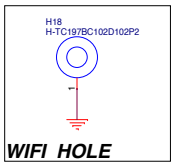
Accelerometer Sensor

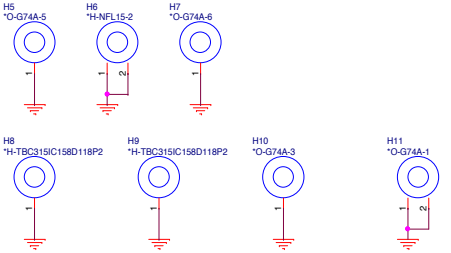


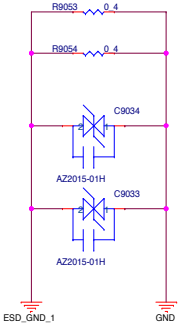
Holes

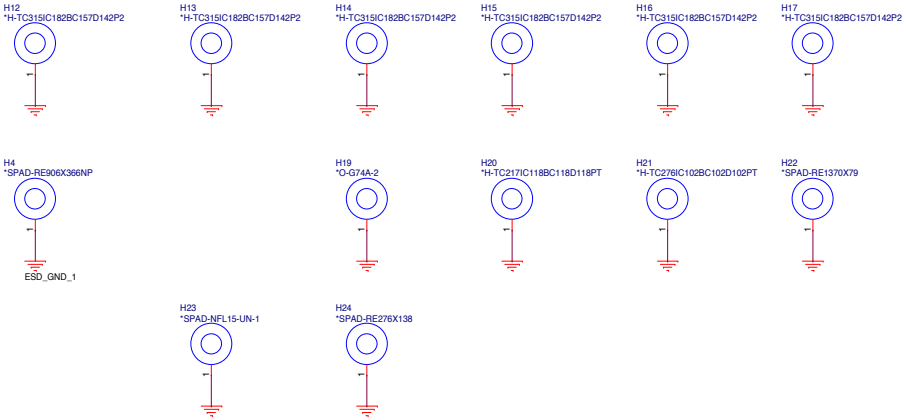


10/17 EMI request









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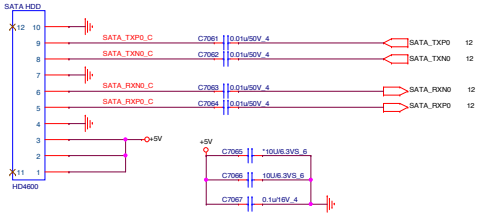
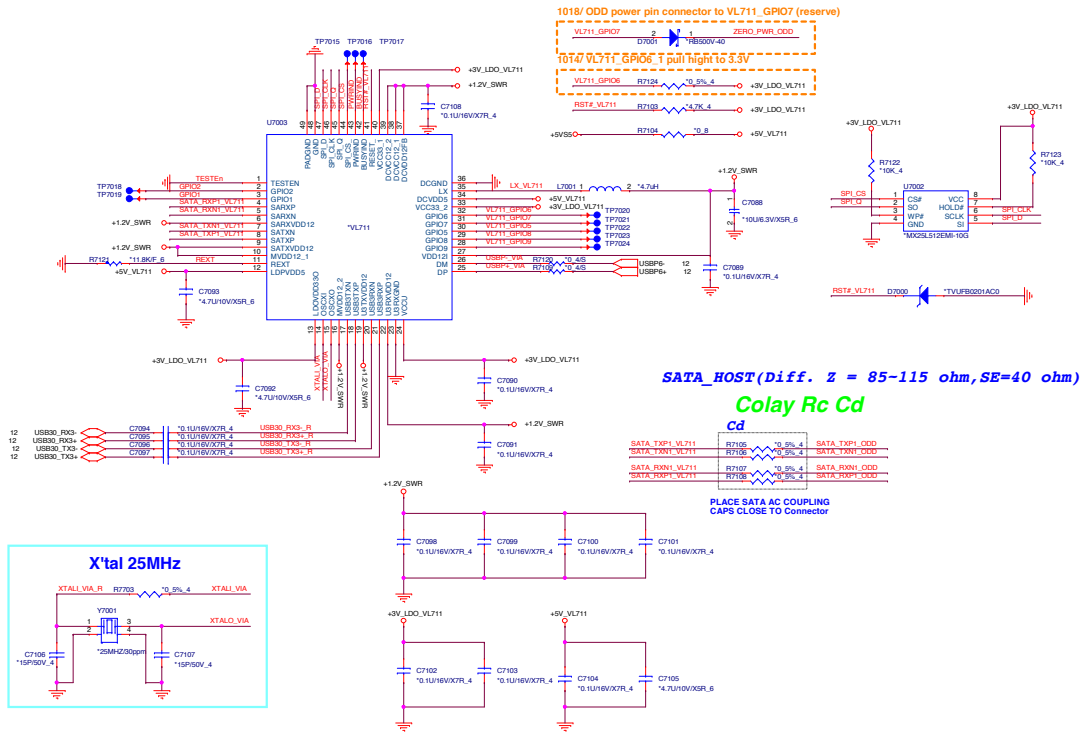
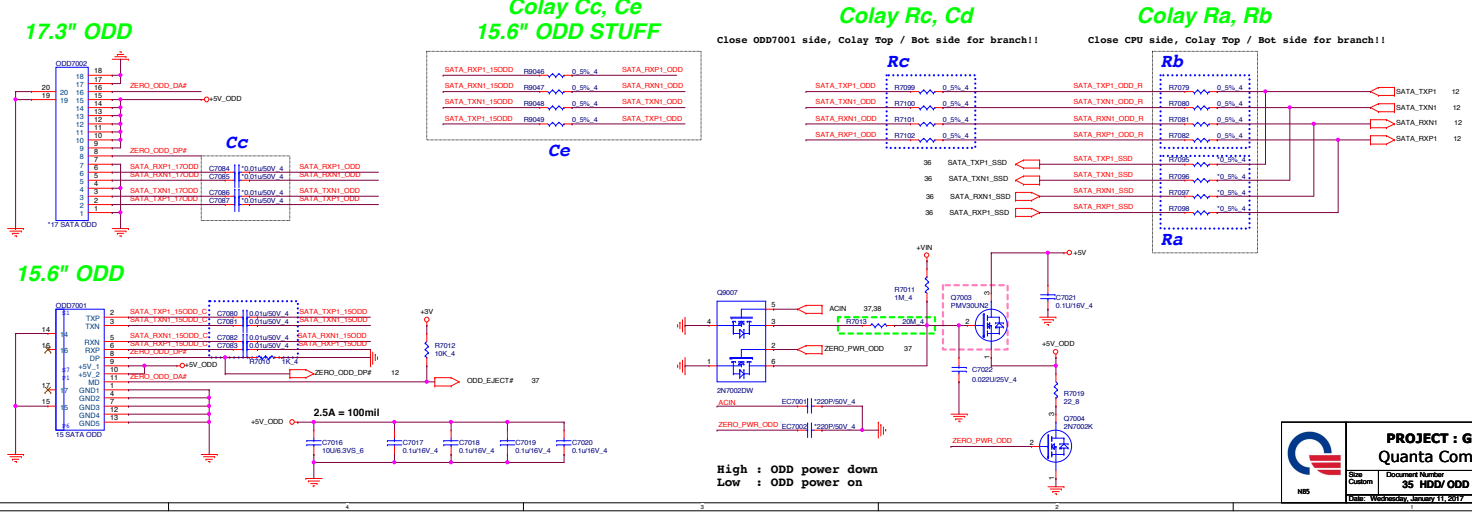
SATA HDD & LED



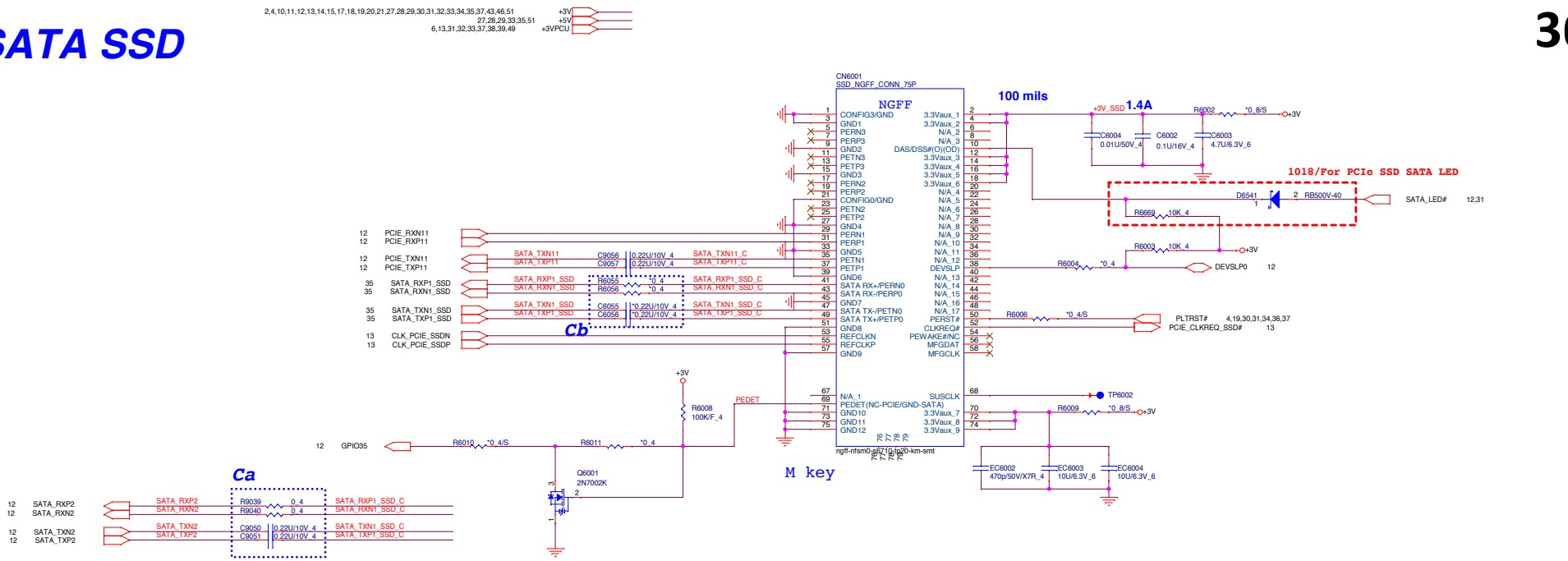
USB3.0 to SATA



SATA ODD

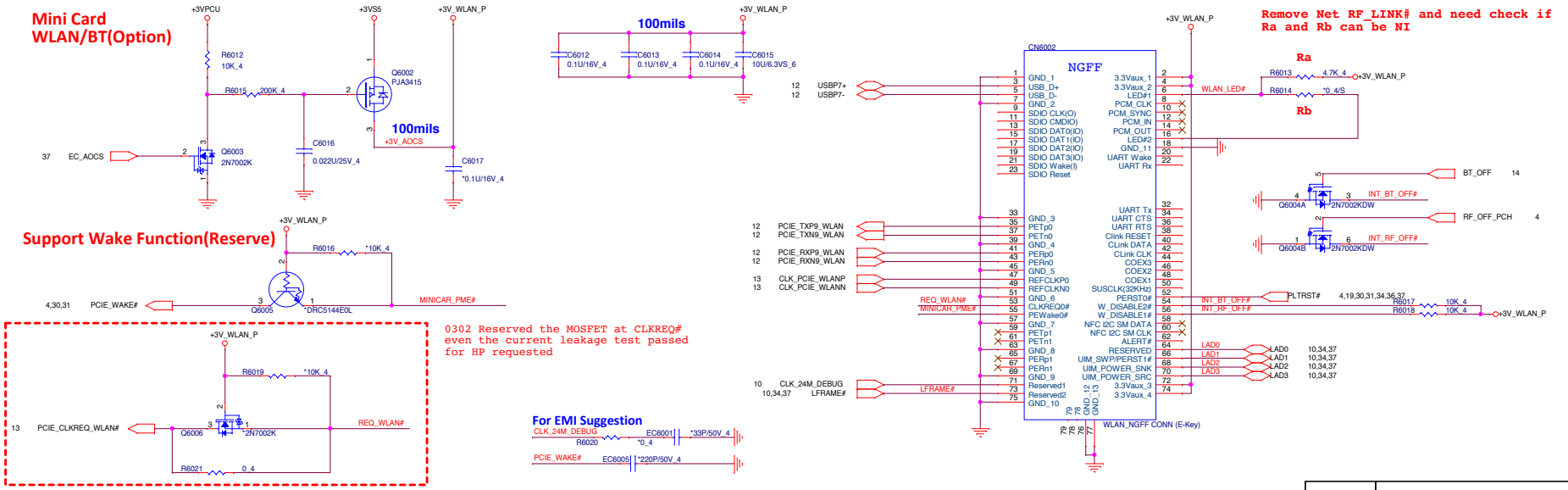


SATA SSD

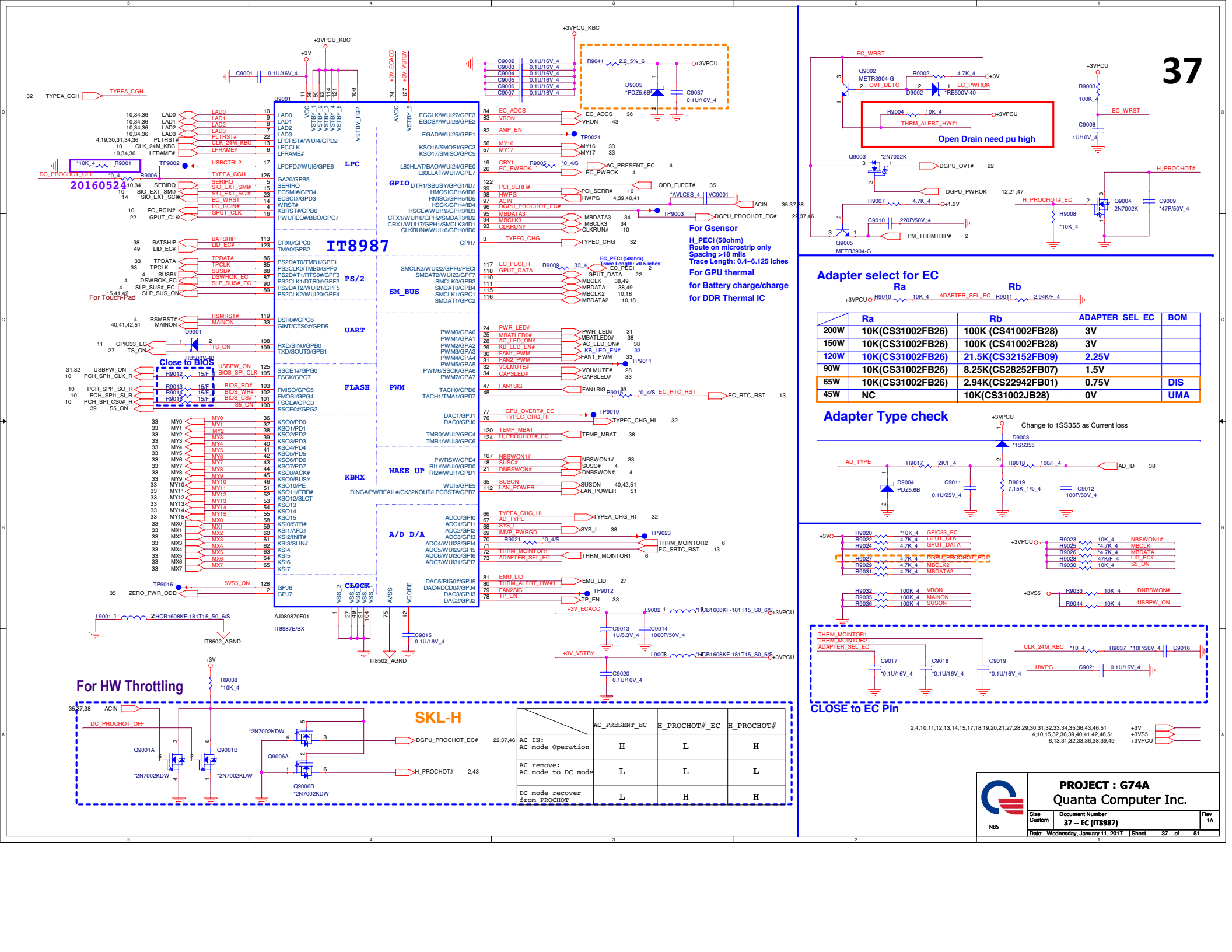


For SATA0 & SATA2 Co-layout Ca, Cb

WLAN



PROJECT : G74A		
Quanta Computer Inc.		
Size: C	Document Number: 36 -- HDD/WLAN(NGFF)	Rev: 1A
Date: Wednesday, January 11, 2017	Sheet 36 of 51	



	AC_PRESENT_EC	H_PROCHOT#_EC	H_PROCHOT#
AC IN: AC mode Operation	H	L	H
AC remove: AC mode to DC mode	L	L	L
DC mode recover from PROCHOT	L	H	H

	Ra	Rb	ADAPTER_SEL_EC	BOM
200W	10K(CS31002FB26)	100K (CS41002FB28)	3V	
150W	10K(CS31002FB26)	100K (CS41002FB28)	3V	
120W	10K(CS31002FB26)	21.5K(CS32152FB09)	2.25V	
90W	10K(CS31002FB26)	8.25K(CS28252FB07)	1.5V	
65W	10K(CS31002FB26)	2.94K(CS22942FB01)	0.75V	DIS
45W	NC	10K(CS31002JB28)	0V	UMA

+3VPCU 6,13,31,32,33,36,37,38,39,49
+5VPCU 28,39,48,51
+BAT_RTC 4,13,15,33,49
+VIN 27,33,35,39,40,41,44,45,46,47,50
+3VPCU 6,13,31,32,33,36,37,38,39,49

ADP=65W

3S1P 41Whr

CN1
51483-00801-V01_Header

N-channel MOS

PQ1 AP0203GMT-HF
PQ2 AON7408
PQ3 AON6414AL

Place this ZVS close to Diode away +VIN

Do Not add test pad on BATDIS_G signal

Place this ZVS close to Far-Far away +VIN

Place this cap close to EC

Place this R&C close to EC

VIN>22.5V (AC OVP)
VIN>17.2V (Enable Charging)
VIN>15.2V (AC present)

Notes:
For 4S pack
Stuff Block A + Ra
Ra = 69.8K (P/N:CS36982FB11)

Vacdet=2.4V

Ra

MIN. BATV=7.2V

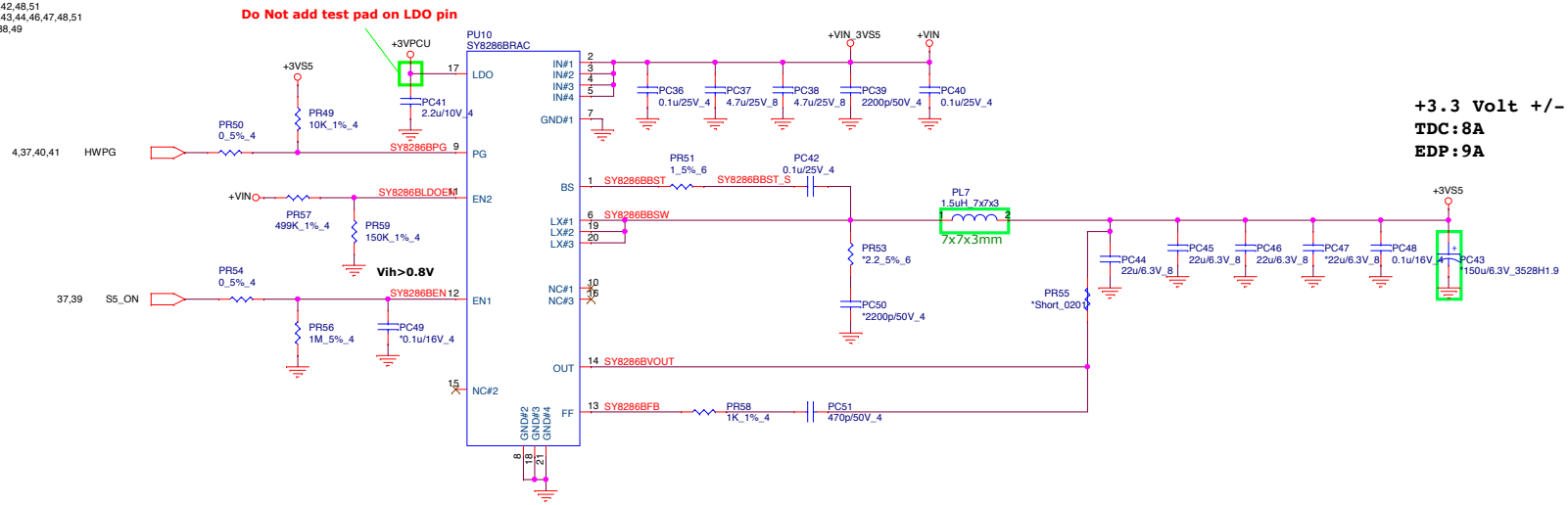
PU9 BQ24738HRGRR

+BAT_RTC SET
BAT= 1S~~~10-ohm
BAT >2S~~~100ohm

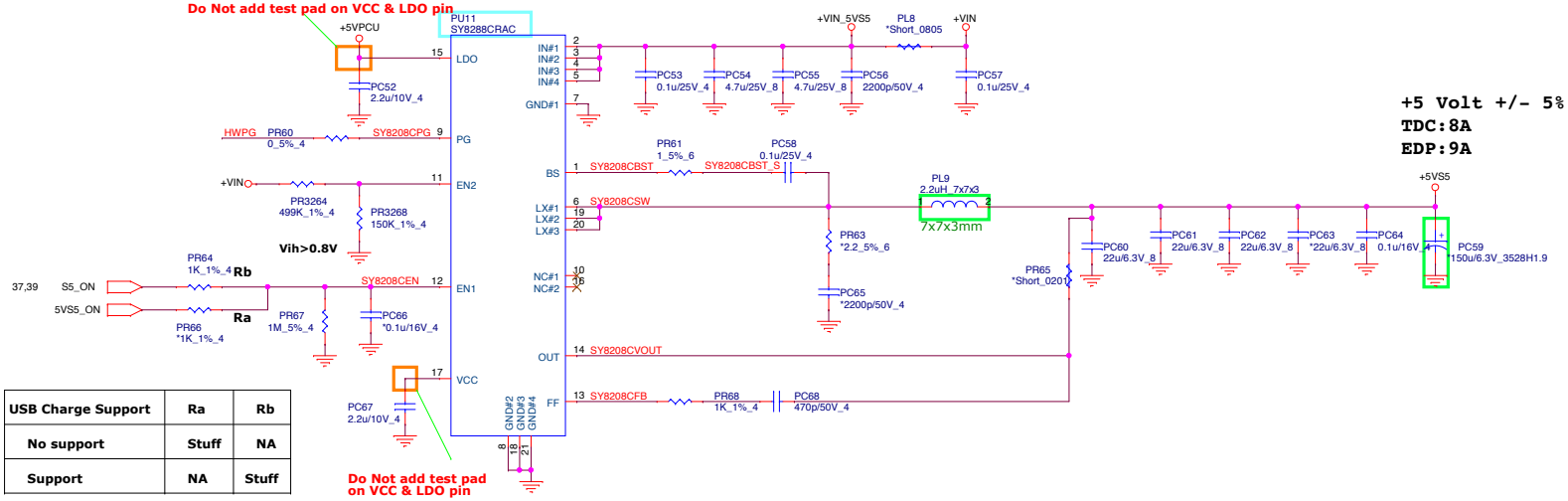
PROJECT : NFLP_KBLU_DR	
Quanta Computer Inc.	
BU5	Size: Custom
Document Number: Charger (BQ24738H)	Rev: 1A
Date: Wednesday, January 11, 2017	Sheet: 38 of 51

DC/DC +3VS5/+5VS5

+VIN 27,33,35,38,40,41,44,45,46,47,50
+3VS5 4,10,15,32,36,37,40,41,42,48,51
+5VS5 4,28,31,32,35,40,41,42,43,44,46,47,48,51
+3VPCU 6,13,31,32,33,36,37,38,49
+5VPCU 28,38,48,51



+3.3 Volt +/- 5%
TDC:8A
EDP:9A



+5 Volt +/- 5%
TDC:8A
EDP:9A

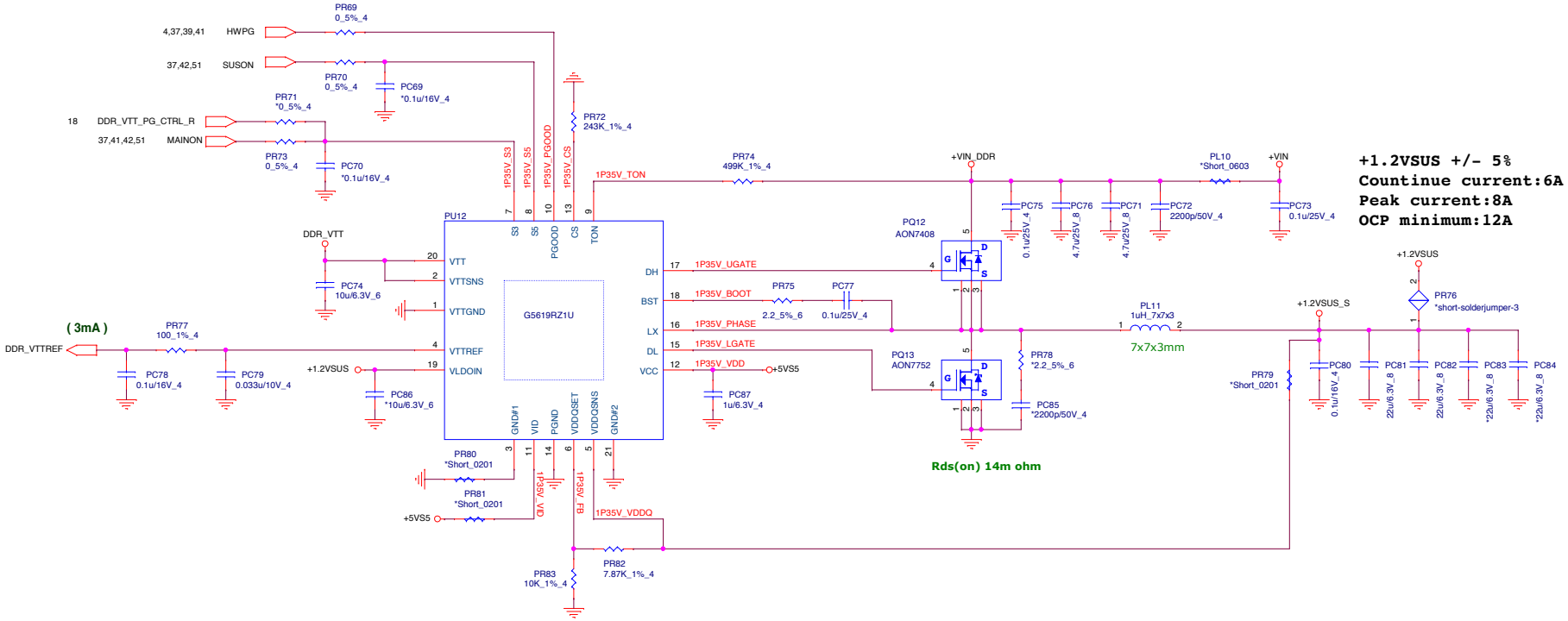
USB Charge Support	Ra	Rb
No support	Stuff	NA
Support	NA	Stuff

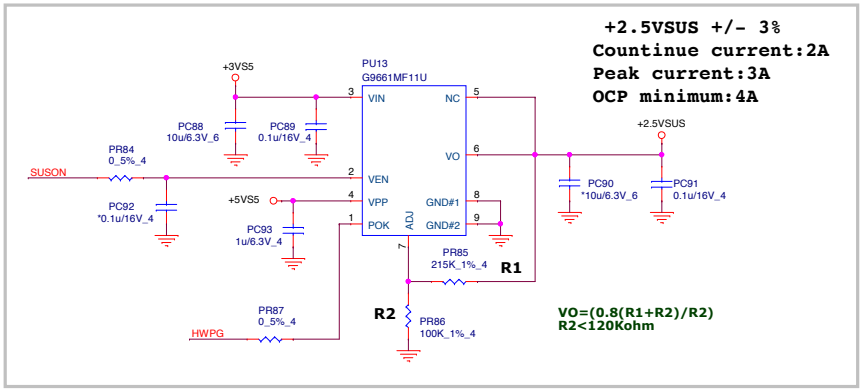
BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	3/5VS5 (SY8208B/SY8208C)	1A
Date: Wednesday, January 11, 2017	Sheet 39 of 51	

+VIN 27,33,35,38,39,41,44,45,46,47,50
+5VS5 4,28,31,32,35,39,41,42,43,44,46,47,48,51
+1.2VSUS 3,6,17,18,42,48
DDR_VTT 17,18



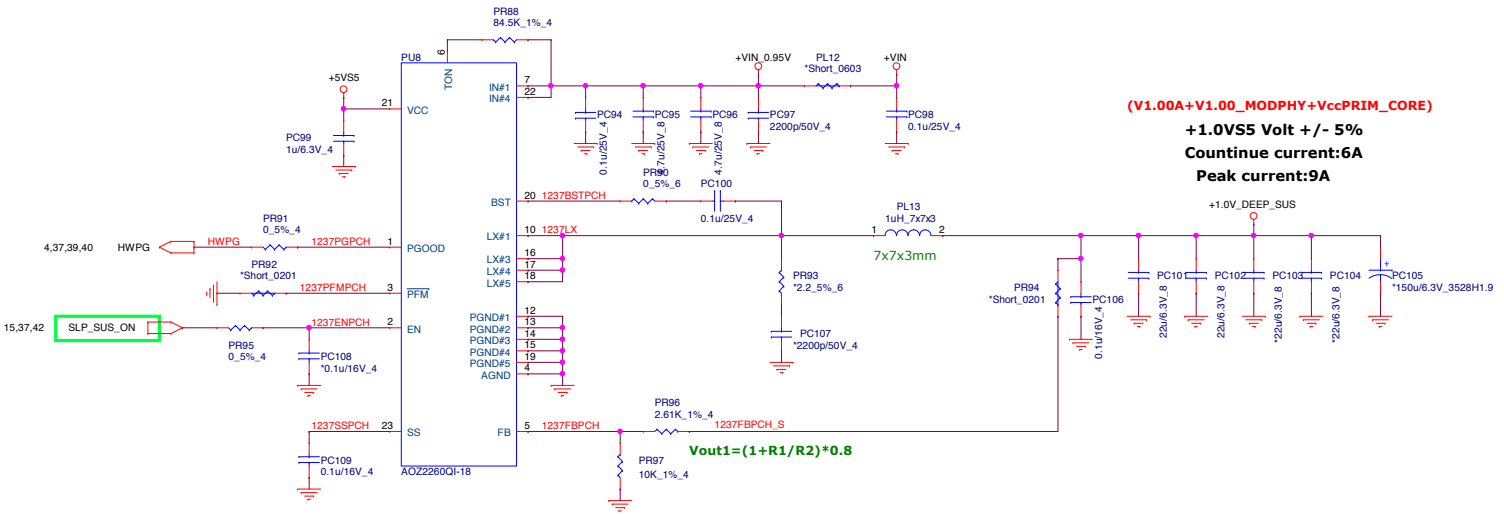


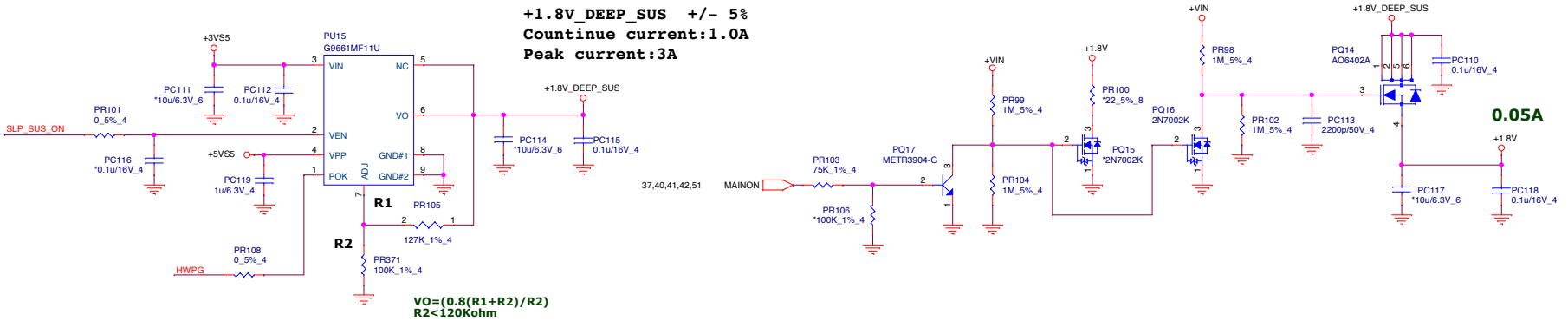
PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
	DDR4 (G5619RZ1U)	1A
Date: Wednesday, January 11, 2017	Sheet 40 of 51	

BU5

+VIN 27,33,35,38,39,40,44,45,46,47,50
+3VS5 4,10,15,32,36,37,39,40,42,48,51
+5VS5 4,28,31,32,35,39,40,42,43,44,46,47,48,51
+1.0V_DEEP_SUS 9,13,15,42
+1.8V_DEEP_SUS 9,15
MAINON 37,40,41,42,51
+1.5V





BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

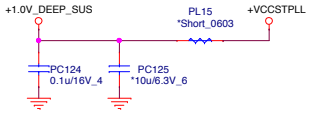
Size	Document Number	Rev
Custom	+1.0V/+1.8V_DEEP_SUS	1A
Date: Wednesday, January 11, 2017	Sheet 41 of 51	

+1.0V 2,4,6,37
+3VS5 4,10,15,32,36,37,39,40,41,48,51
+5VS5 4,28,31,32,35,39,40,41,43,44,46,47,48,51
+VCCIO 2,6
+1.2VSUS 3,6,17,18,40,48
+VCCSTPLL 2,4,5,6,9,43
+1.0V_DEEP_SUS 9,13,15,41
+1.2V_VCCPLL_OC 6
MAINON 37,40,41,51

Volume Segment
Vcc_ST: 0.12A
Vcc_PLL: 0.12A

<= 10ms, full load ready
(Vcc_ST+Vcc_PLL)

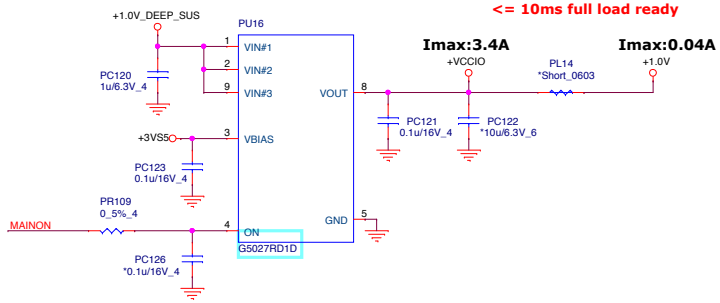
Imax:0.24A

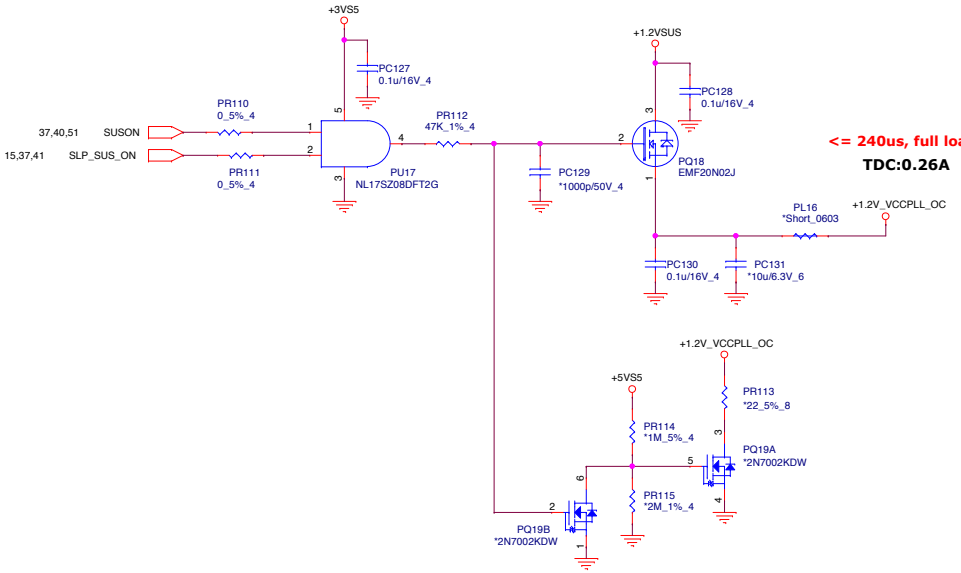


Volume Segment
Vcc_STG: 0.04A
Vcc_IO: 3.4A

<= 10ms full load ready

Imax:3.4A **Imax:0.04A**





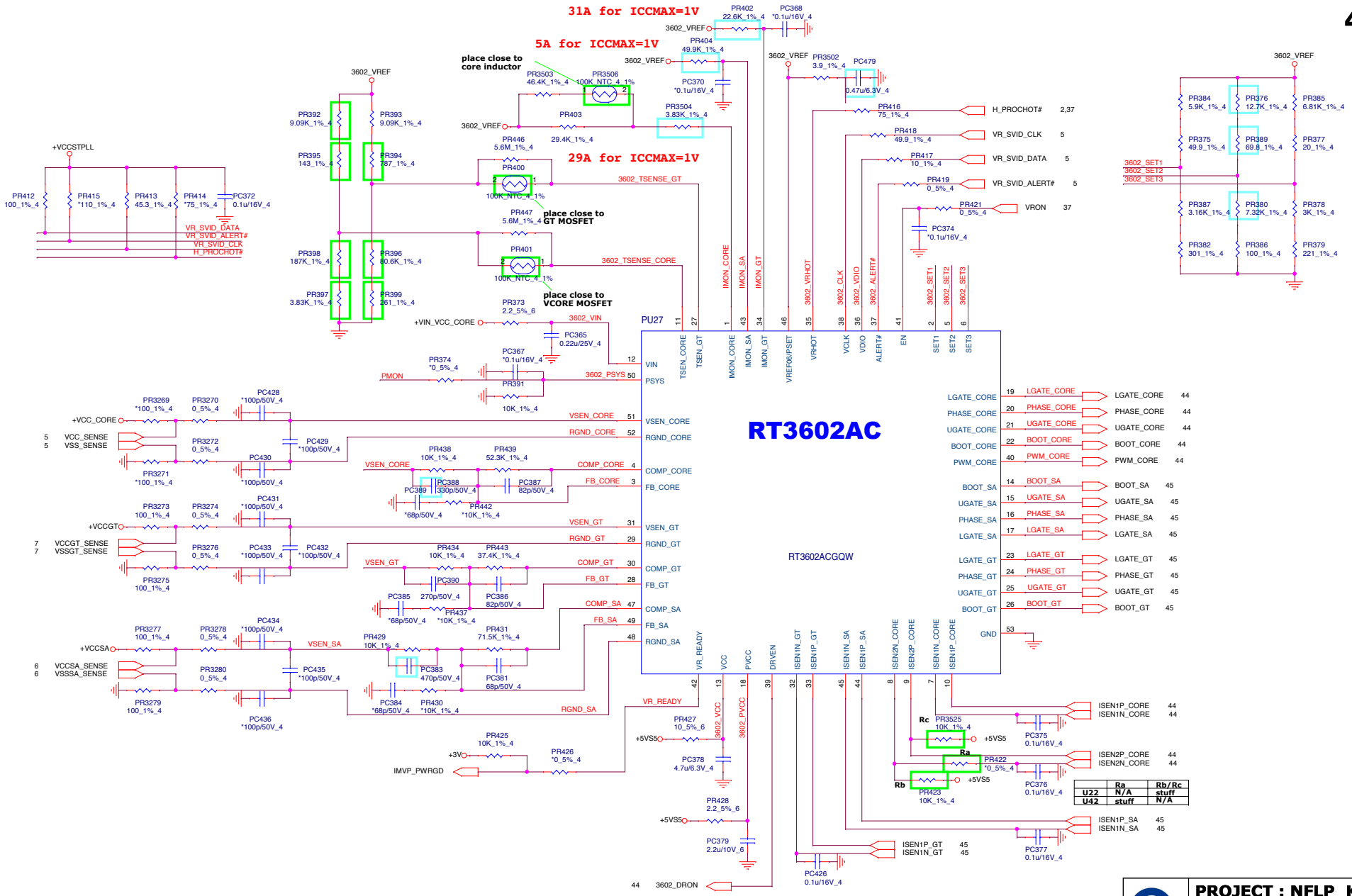
<= 240us, full load ready
TDC:0.26A

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

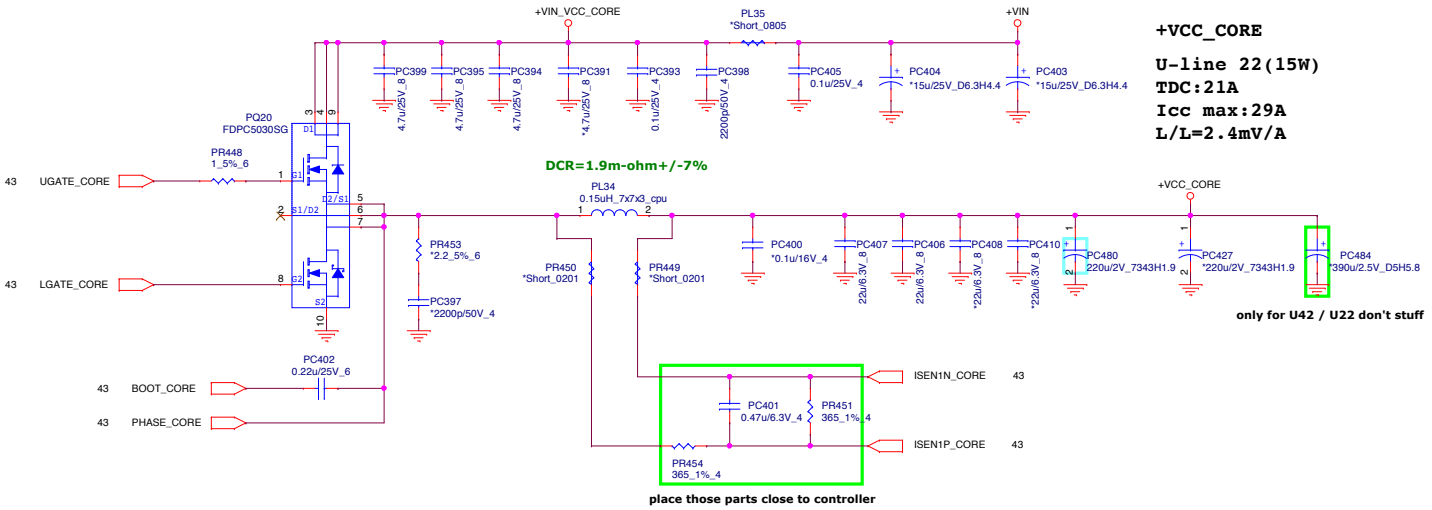
BU5

Size	Document Number	Rev
Custom	+1.0V/+VCCSTPLL	1A

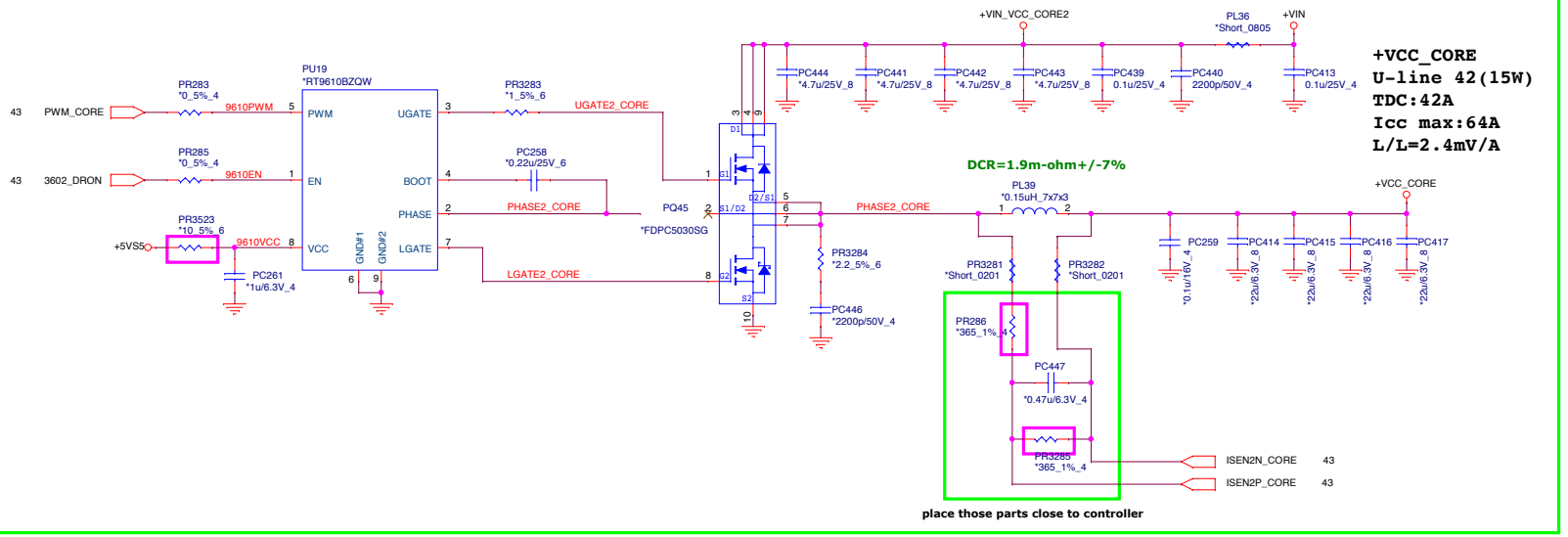
Date: Wednesday, January 11, 2017 Sheet 42 of 51


31A for ICCMAX=1V
5A for ICCMAX=1V
29A for ICCMAX=1V
place close to core inductor
place close to GT MOSFET
place close to VCORE MOSFET
RT3602AC
RT3602ACGQW
PU27
+VCCSTPLL
3602_VREF
+VIN_VCC_CORE
PMON
+VCC_CORE
+VCCGT
+VCCSA
+3V
+5VS5
IMVP_PWRGD
3602_DRON
H_PROCHOT#
VR_SVID_CLK
VR_SVID_DATA
VR_SVID_ALERT#
VRON
3602_SET1
3602_SET2
3602_SET3
VCC_SENSE
VSS_SENSE
VCCGT_SENSE
VSSGT_SENSE
VCCSA_SENSE
VSSSA_SENSE
VIN
PSYS
VSEN_CORE
RGND_CORE
COMP_CORE
FB_CORE
VSEN_GT
RGND_GT
COMP_GT
FB_GT
VSEN_SA
RGND_SA
COMP_SA
FB_SA
VR_READY
VCC
PVCC
DRVEN
GND
LGATE_CORE
PHASE_CORE
UGATE_CORE
BOOT_CORE
PWM_CORE
BOOT_SA
UGATE_SA
PHASE_SA
LGATE_SA
LGATE_GT
PHASE_GT
UGATE_GT
BOOT_GT
ISEN1P_CORE
ISEN1N_CORE
ISEN2P_CORE
ISEN2N_CORE
ISEN1P_SA
ISEN1N_SA
ISEN1P_GT
ISEN1N_GT
IMON_CORE
IMON_SA
IMON_GT
VREF06/PSET
VRHOT
VCLK
VDIO
ALERT#
EN
SET1
SET2
SET3
3602_TSENSE_GT
3602_TSENSE_CORE
3602_VIN
3602_PSYS
3602_VCC
3602_PVCC
3602_CLK
3602_VDIO
3602_ALERT#
Rc
Ra
Rb
U22
U42
PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.
BU5
CPU VR IC (RT3602AC)
Wednesday, January 11, 2017

+VIN 27,33,35,38,39,40,41,45,46,47,50
+5VS5 4,28,31,32,35,39,40,41,42,43,46,47,48,51



For U42 --> Add These Components



+VCC_CORE
U-line 22(15W)
TDC:21A
Icc max:29A
L/L=2.4mV/A

+VCC_CORE
U-line 42(15W)
TDC:42A
Icc max:64A
L/L=2.4mV/A

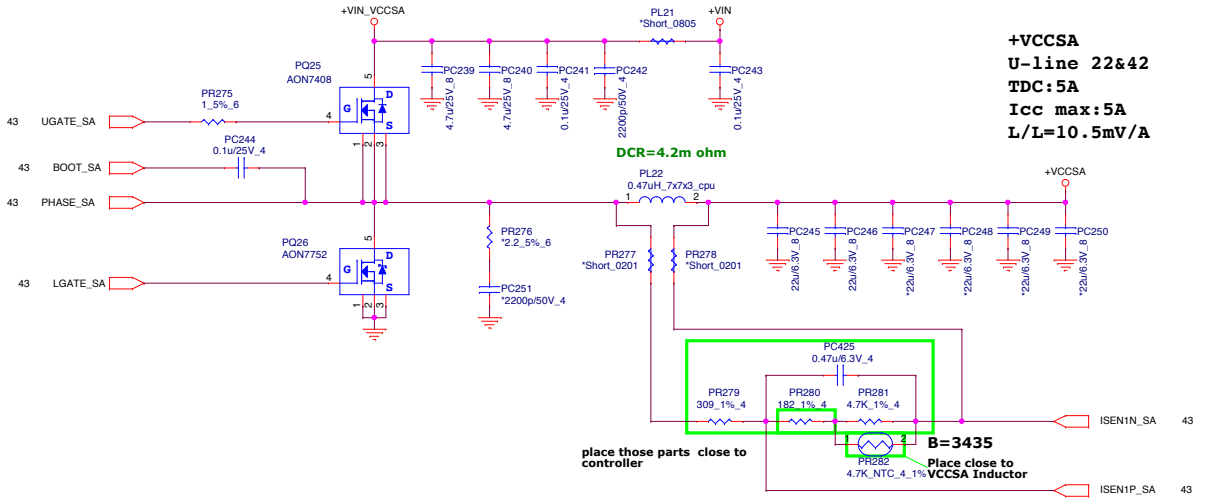
BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

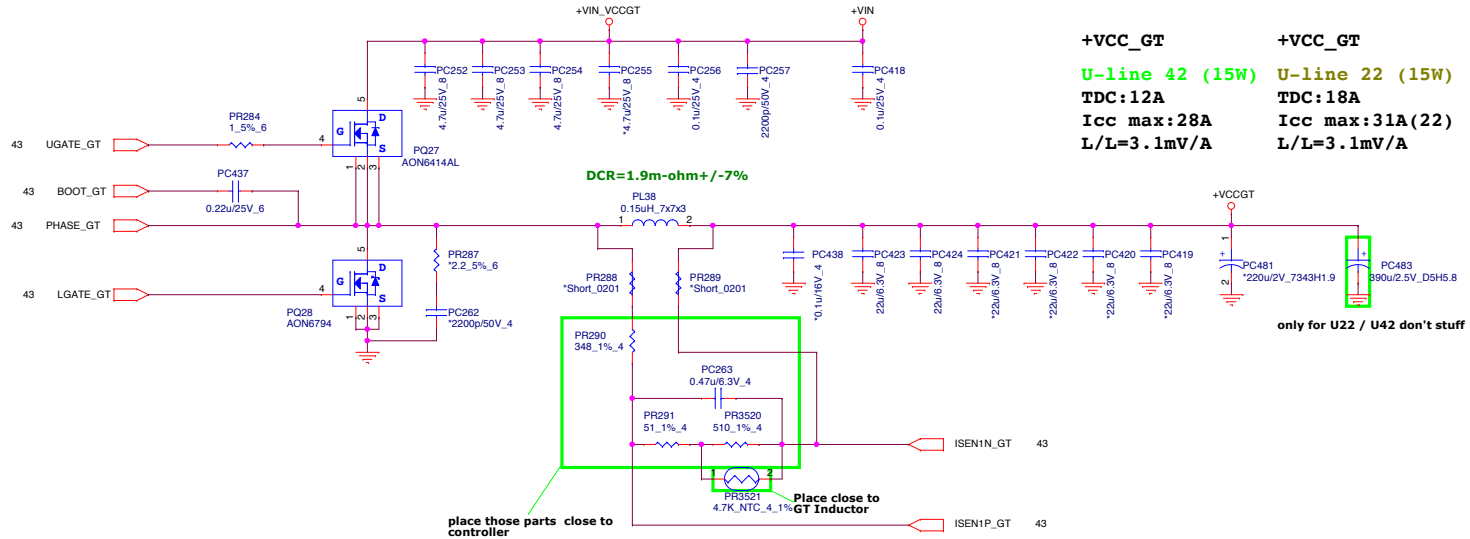
Size	Document Number	Rev
Custom	+VCCSA (NCP81253)	2A

Date: Wednesday, January 11, 2017 Sheet 44 of 51

+VIN 27,33,35,38,39,40,41,44,46,47,50
+5VS5 4,28,31,32,35,39,40,41,42,43,44,46,47,48,51
+VCCSA 6,43
+VCCGT 7,43



+VCCSA
U-line 22&42
TDC:5A
Icc max:5A
L/L=10.5mV/A



+VCC_GT
U-line 42 (15W)
TDC:12A
Icc max:28A
L/L=3.1mV/A

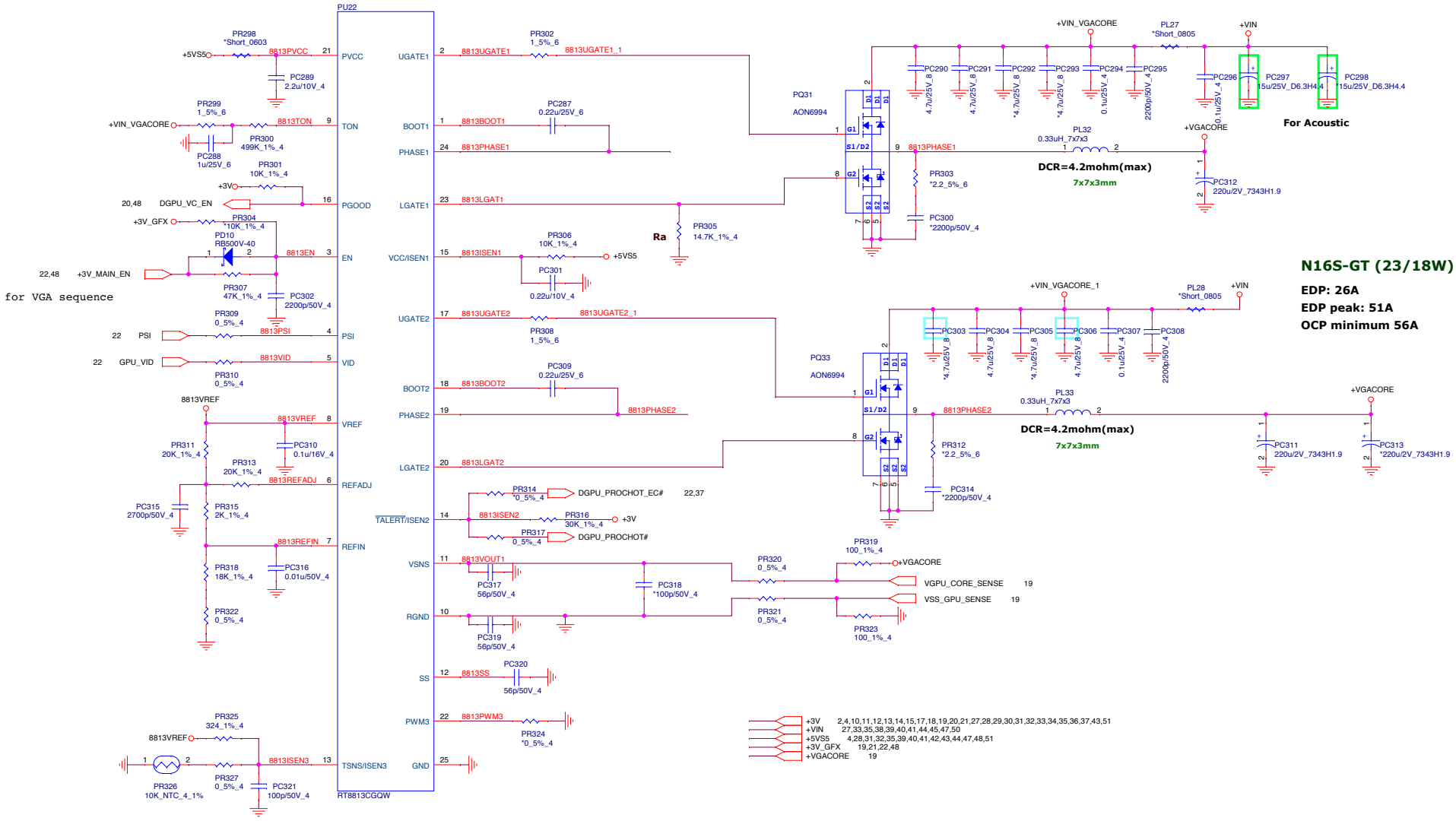
+VCC_GT
U-line 22 (15W)
TDC:18A
Icc max:31A(22)
L/L=3.1mV/A

BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VCCSA (NCP81253)	2A
Date: Wednesday, January 11, 2017	Sheet 45 of 51	

VGA Core



N16S-GT (23/18W)

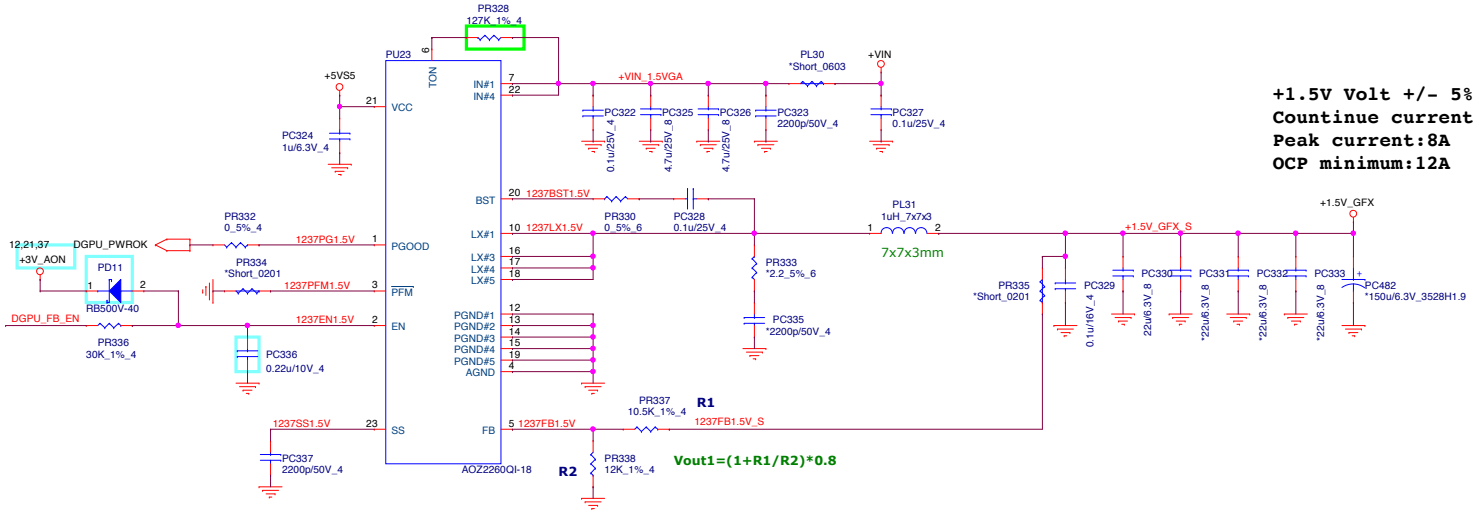
EDP: 26A

EDP peak: 51A

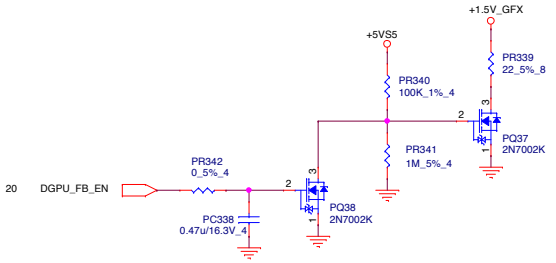
OCP minimum 56A

BU5	**PROJECT : NFLP_KBLU_DR** Quanta Computer Inc.	
Size: Custom	Document Number: +VGACORE (RT8813C)	Rev: 2A
Date: Wednesday, January 11, 2017	Sheet 46 of 51	

+VIN 27,33,35,38,39,40,41,44,45,46,50
+5VS5 4,28,31,32,35,39,40,41,42,43,44,46,48,51
+1.5V_GFX 20,21,23,24,25,26



+1.5V Volt +/- 5%
Countinue current:6A
Peak current:8A
OCP minimum:12A



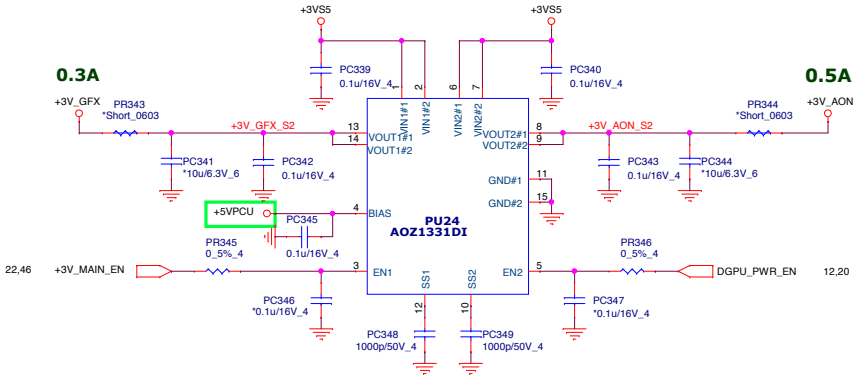
PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

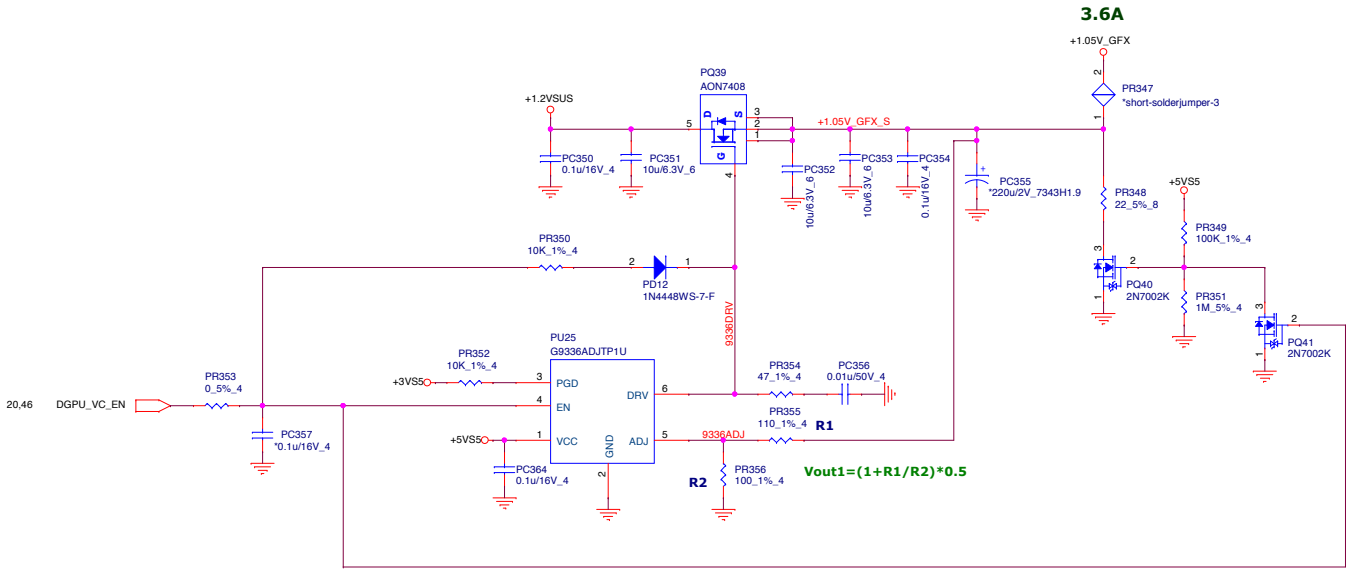
Size	Document Number	Rev
Custom	+1.5V_GFX (AOZ2260QI-18)	1A

BU5

Date: Wednesday, January 11, 2017 | Sheet 47 of 51

+VIN 27,33,35,38,39,40,41,44,45,46,47,50
+3VS5 4,10,15,32,36,37,39,40,41,42,51
+5VS5 4,28,31,32,35,39,40,41,42,43,44,46,47,51
+3V_GFX 19,21,22,46
+3V_AON 19,22,47
+1.2VSUS 3,6,17,18,40,42
+1.05V_GFX 19,20,21



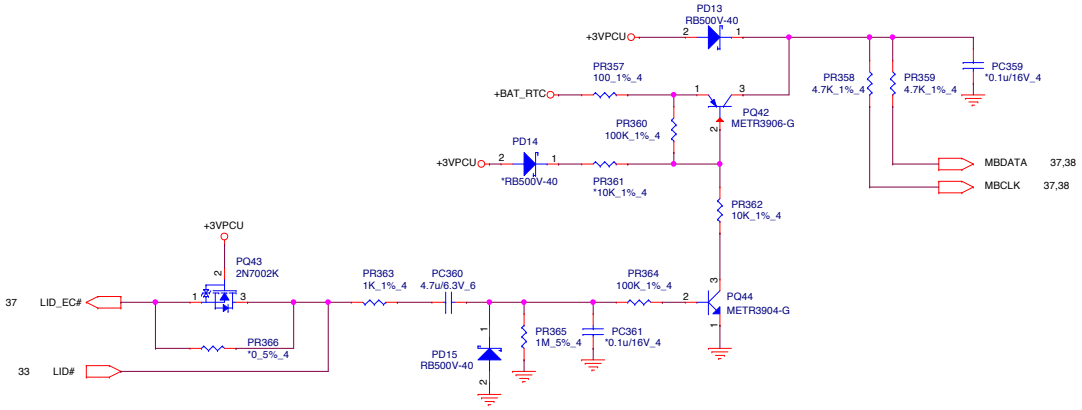


BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+3V/+1.05V_GFX(APL3523A)	1A
Date: Wednesday, January 11, 2017	Sheet 48 of 51	

+3VPCU 6,13,31,32,33,36,37,38,39
+BAT_RTC 4,13,15,33,38

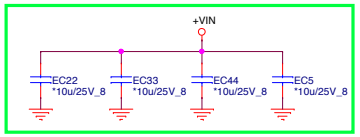


BU5

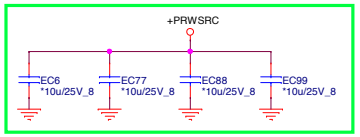
PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LID SW for storage mode	1A
Date: Wednesday, January 11, 2017	Sheet 49 of 51	

EMI request for ISN



EMI request for ISN

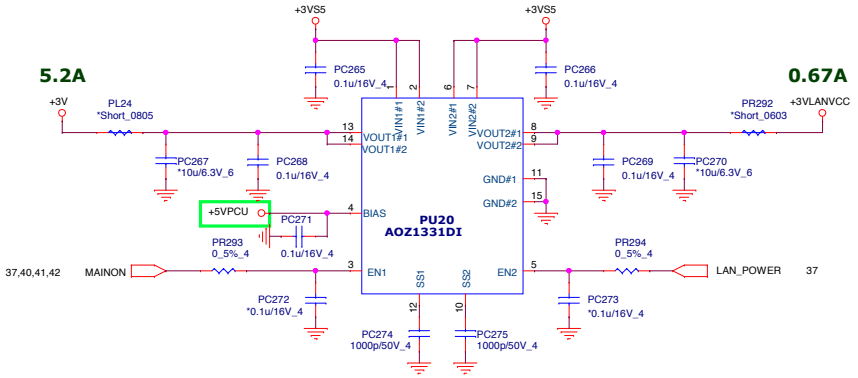


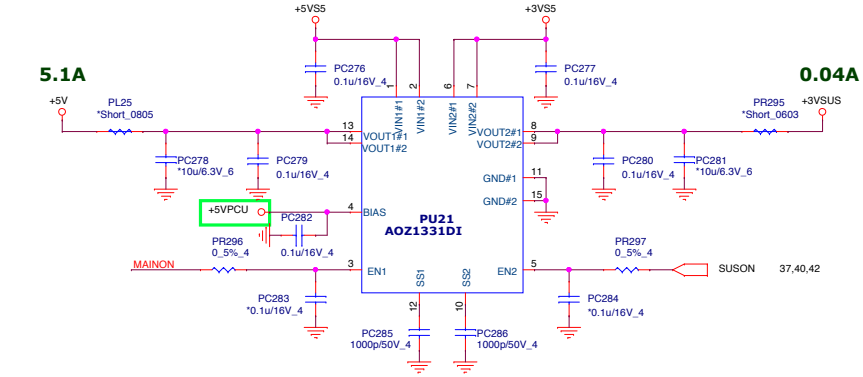
BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	**EMI solution**	1A
Date: Wednesday, January 11, 2017	Sheet 50 of 51	

+3V 2,4,10,11,12,13,14,15,17,18,19,20,21,27,28,29,30,31,32,33,34,35,36,37,43,46
+5V 27,28,29,33,35
+VIN 27,33,35,38,39,40,41,44,45,46,47,50
+3VS5 4,10,15,32,36,37,39,40,41,42,48
+5VS5 4,28,31,32,35,39,40,41,42,43,44,46,47,48
+3VSUS 33
+5VPCU 28,38,39,48
+3VLANVCC 30





BU5

PROJECT : NFLP_KBLU_DR
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Load switch IC (APL3523A)	1A

Date: Wednesday, January 11, 2017 | Sheet 51 of 51